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DDP-516-21
DIRECT MEMORY ACCESS
Option Manual

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DIVISION

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DDP-516-21
DIRECT MEMORY ACCESS OPTION

INTRODUCTION

This document contains a detailed description of the Direct Memory Access (DMA) option.

Reference Data

Instruction Manual for DDP-516 General Purpose Computer: Volume I, 3C Doc. No. 130071620; Volume II, 3C Doc. No. 130071621; Volume III, 3C Doc. No. 130071622.

Functional Description

The DMA provides a direct, high-speed path for an external device to computer memory for up to four channels. The DMA word-transfer-rate approaches 0.9 μs and is capable of addressing up to 32K of memory.

To effect a transfer, the DMA causes computer breaks between cycles without regard to end of instruction. The initiation and termination of the DMA cycle is controlled by the external device request lines.

INSTALLATION

The DMA is contained in two bays, one of which is the main frame (unit A). The DMA logic in the main-frame bay is located in fixed positions as shown on LBD No. 248. The DMA logic external to the main frame is a relocatable 2x3 BLOC, whose PAC allocations are shown on LBD No. 249. DMA cable No. 1 transfers the address counter lines (ACTXX) to the CPU Y-register.

INSTRUCTION COMPLEMENT

DMA instructions are for loading the address and range counters and for reading the contents of the range counters.

Load Address Counter Channel 1, SMK '0124

This instruction has the following function:

$$(0) \rightarrow (AC1)_{1-16} \mid (A)_{1-16} \rightarrow (AC1)_{1-16} \mid (0) \rightarrow (RC1)_{1-16}$$

The contents of A are the address of the memory location to be accessed by the first DMA cycle for channel 1. Note that the load-address instruction clears the range counter and should therefore precede the load-range instruction.

Load Address Counter Channel 2, SMK '0224

This instruction is the same as SMK '0124 except that it is for Channel 2.

Load Address Counter Channel 3, SMK '0324

This instruction is the same as SMK '0124 except that it is for Channel 3.

Load Address Counter Channel 4, SMK '0424

This instruction is the same as SMK '0124 except that it is for Channel 4.

Load Range Counter Channel 1, SMK '1124

This instruction has the following function:

$$(A)_{2-16} \rightarrow (RC1)_{2-16}$$

The contents of A are the two's complement of the number of transfers to be accomplished. Note that RC must be cleared previously by an SMK '0X24 (load address counter) instruction so that the transfer count is not altered when loaded into the range counter. (Essentially, the contents of A are inclusively-ORed with the contents of RC.)

Load Range Counter Channel 2, SMK '1224

This instruction is the same as SMK '1124 except that it is for Channel 2.

Load Range Counter Channel 3, SMK '1324

This instruction is the same as SMK '1124 except that it is for Channel 3.

Load Range Counter Channel 4, SMK '1424

This instruction is the same as SMK '1124 except that it is for Channel 4.

Read Range Counter Channel 1, INA '1124

This instruction functions as follows.

If (RC) = 0: NOP and execute next sequential instruction
If (RC) ≠ 0: (0)→ (A) | (RC) → (A) | skip next sequential instruction

Read Range Counter Channel 2, INA '1224

Instruction INA '1224 is the same as INA '1124 except that INA '1224 is for Channel 2.

Read Range Counter Channel 3, INA '1324

Instruction INA '1324 is the same as INA '1124 except that INA '1324 is for Channel 3.

Read Range Counter Channel 4, INA '1424

Instruction INA '1424 is the same as INA '1124 except that INA '1424 is for Channel 4.

THEORY OF OPERATION

Functional Areas (See Figure 1)

Control Logic. -- The DMA control logic (LBD No. 241) contains the priority network (PN) for determining the priority of the active DMA requests (DILAX) and the logic for initiating and controlling the DMA cycle.

Timing Level Generator. -- The DMA Timing Level Generator (LBD No. 240) generates the various timing levels required for a DMA cycle. A DMA request (DMARQ) enables the CPU master clock oscillator outputs MCSET, MCRST, and MTLG, to trigger the DMA timing level flip-flops. There are five of these flip-flops: TLAFF, TLBFF, TLCFF, TLDFF, and TLEFF. See Figure 2 which shows the level sequence if only one DMA cycle is required. The transition from one level to the next is controlled by the TACFF, TBCFF, and SAMIN flip-flops. Note that the TL4FF flip-flop (LBD No. 118) is inhibited while the DMA timing level generator is enabled.

If two or more DMA cycles occur in succession, timing levels TLA and TLE occur simultaneously except at the beginning of the first cycle when only TLA is generated and the end of the last cycle when only TLE is generated. The levels for two or more successive DMA cycles are generated as shown below.

Start DMA

TL3	TLA	TLB	TLC	TLD	TLE· TLA	TLB	TLC	TLD	TLE· TLA	TLB	TLC	TLD	TLE	TL4

Repeat N Times

End DMA

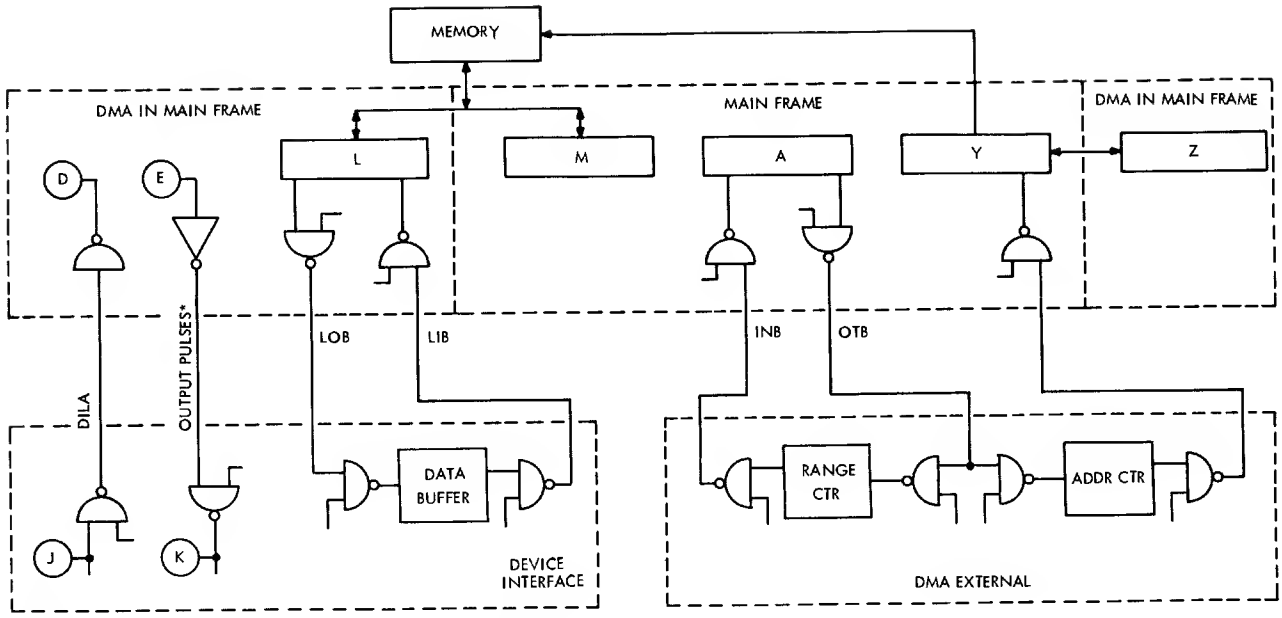


Figure 1. CPU/DMA/External Device Interface Block Diagram

L-Register. -- The L-register (LBDs No. 242 and 243) is the memory buffer register. All transfers to and from memory occur through the L-register.

Z-Register. -- The Z-register (LBD No. 244) provides storage for the contents of the Y-register during the DMA cycle while the DMA is using the Y-register.

Address Counter (AC). -- Each channel has a 16-bit address counter (LBDs No. 251, 253, 255) which stores DMA cycle starting address and the read/write control bit. The highest order bit (bit 1) position of AC stores the read/write control. A ONE specifies a write cycle (input mode) and a ZERO specifies a read cycle (output mode). The address contents of AC (bits 2 through 16) are incremented once each cycle to provide the address for the next cycle.

Range Counter (RC). -- Each channel has a 16-bit range counter (LBDs No. 252, 254, 256) which stores the two's complement of the number of transfers to take place. The contents of RC are incremented once each cycle. When RC equals all ONEs an end of range signal (ERCHX) is delivered to the external device signifying that the required number of transfers has been accomplished.

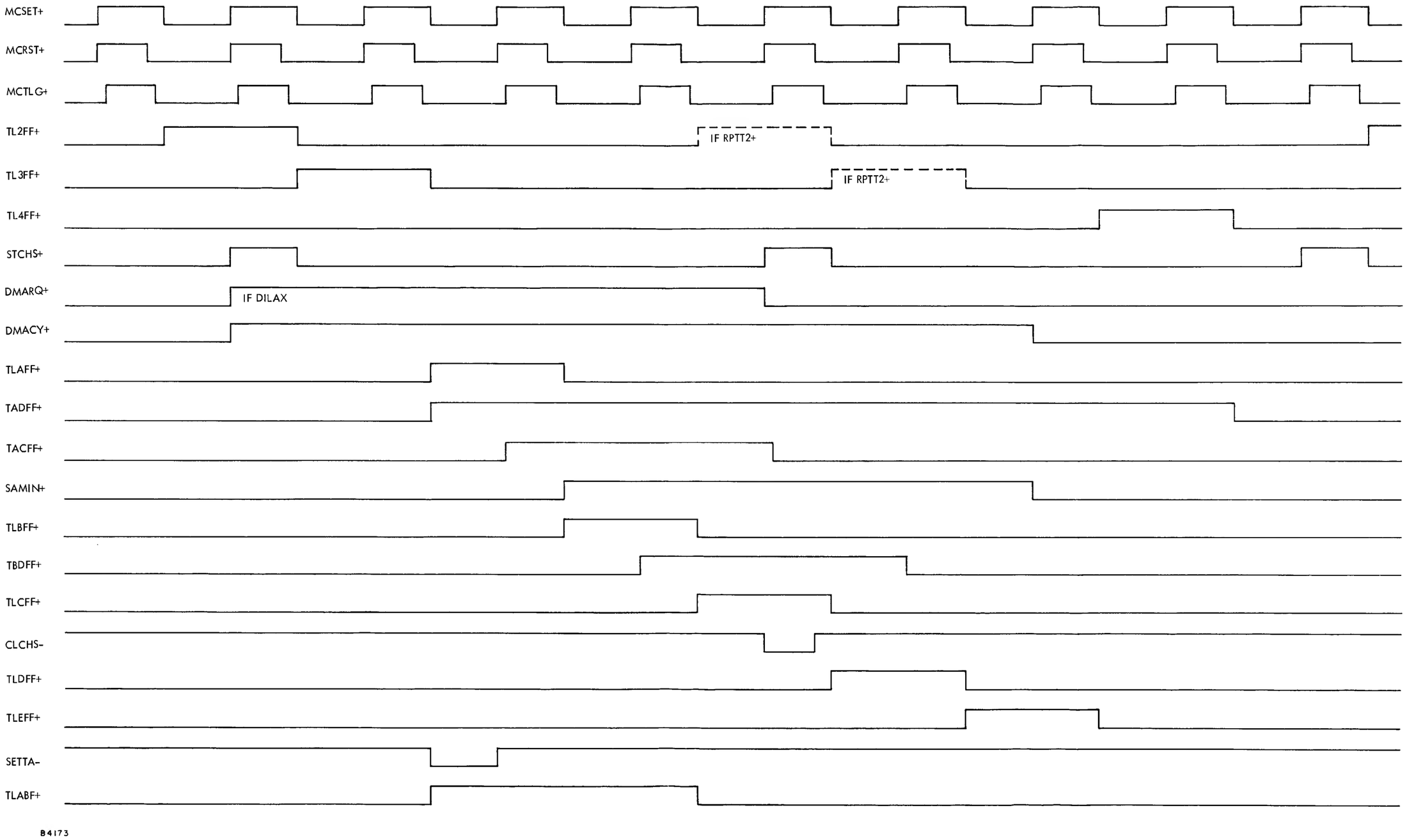


Figure 2. Timing Levels and Primary Control Signals for One DMA Cycle

SMK and INA Instruction Logic

For SMK load AC or RC instruction, the address bus lines (ADBXX) are sent to a decoder (LBD No. 250-B9). The decoder outputs (OTPAX or OTPRX) specify a particular address counter (AC) or range counter (RC). Note that a load AC SMK instruction should be executed before a load RC for the same channel because the load AC SMK clears both the AC and RC. The load RC SMK clears neither of these counters. For example, when a load AC SMK '0X24 is executed, the decoder output OTPAX is gated with CMKXX (LBD No. 134-K7) to generate CLARX (LBDs No. 251, 253, 255-D10). CLARX clears the AC and RC for that channel. On the trailing edge of CMKXX, the OTPAX flip-flop (LBDs No. 251, 253, 255-G11) is set to gate the output bus (OTBXX) onto the SAXXX lines. The SAXXX lines then set the AC stages. At the end of the instruction, when signal SMKXX goes false, the OTPAX flip-flop is DC reset, thereby preventing the OTBXX lines from affecting the counter. For a load RC instruction (for example SMK '1X24), an OTPRX decoder output enables the OTBXX lines to the proper range counter.

An INA instruction is decoded by a gate (LBDs No. 252, 254, 256-D11) whose output enables the contents of RC (RCXXX) to the input bus (INBXX). The INA also enables ERLAX (indicates RC contains all ZEROs) to generate DRLIN. The state of DRLIN determines whether the INA is to be treated as a NOP or the contents of RC are transferred to the A-register and the next sequential instruction is to be skipped.

DMA Cycle

For a detailed DMA cycle description, see DMA cycle flow chart (Figure 3) and flow chart analysis. The DMA logic is shown on LBDs No. 240 through 245 and 248 through 259. DMA-external-device timing is shown in Figure 4. The DMA mnemonics are defined in the function index list.

A DMA cycle is activated by an external device request. The priority network (PN) logic determines the request priority and enables the proper channel logic. The DMA cycle begins at the trailing edge of TL3. It inhibits TL4 and begins generation of its own timing signals. Every TL1 the contents of Y are transferred to Z for preservation in case of a DMA cycle. The DMA cycle starts a memory cycle which is a read or write cycle depending on the state of the DMAWR flip-flop. The Y-register is cleared and the contents of address counter (AC) representing the address to be accessed in the first DMA cycle are placed in Y. AC is then incremented to form the address for the next DMA cycle. For a read cycle, the contents of the addressed memory location are inhibited from the M-register and placed in the L-register. The L-register is then transferred to the LOBXX lines and from thence to the external device. For a write cycle, the external device data is transferred from the external device to the L-register via the LIBXX lines and from the L-register to the addressed memory location.

If end of range (RC equals all ONEs) is reached, the external device disables its request line and transfers for this channel are terminated. The contents of RC are then incremented. The DMA again searches its request lines. If any are active, it causes another DMA cycle. If no requests exist, the DMA returns control to the CPU and enables TL4.

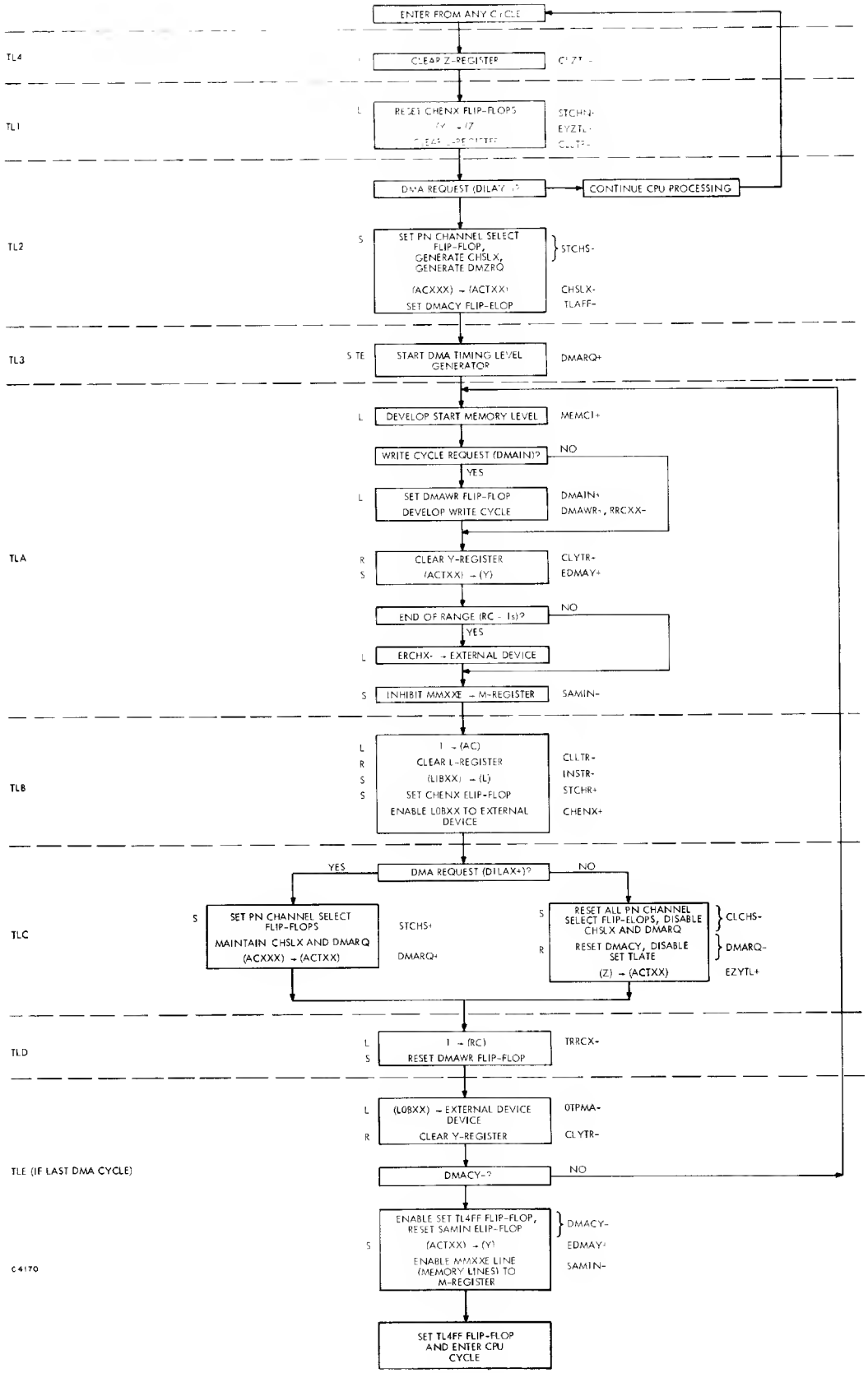


Figure 3. DMA Cycle Flow Chart

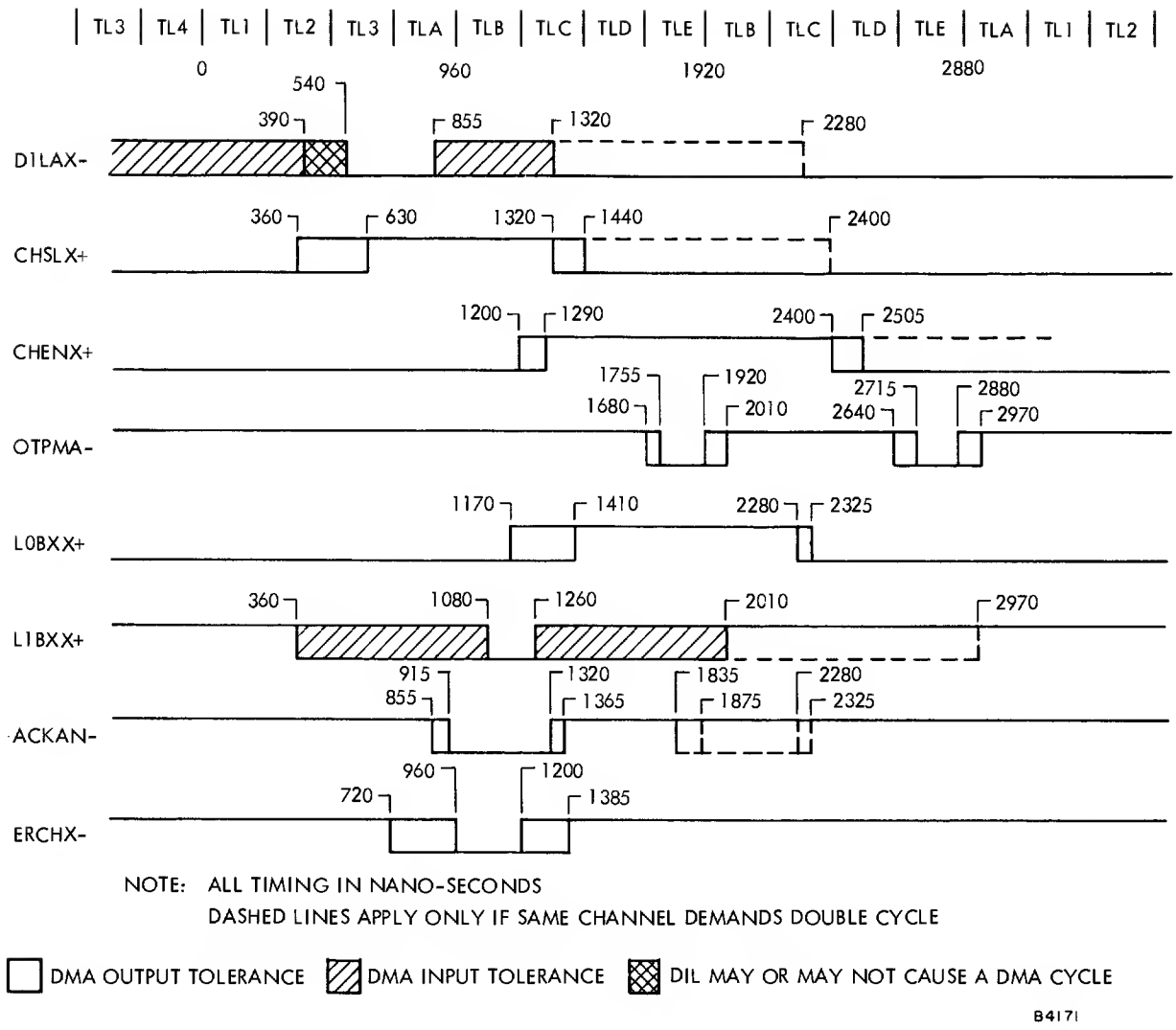


Figure 4. DMA/External Device Interface Timing

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
CLZTL-	241-L5	CPU	TL4	L	(TL4FF+)	241-L5	244-A3/D2/ F3/J2	Clears Z-register
STCHN+	241-L1	CPU	TL1	L	(TL1FF+)	241-L1	241-A7/A9/ C7/C9	Resets CHFNX flip-flops
EYZTL+	241-L6	CPU	TL1	L	(TL1FF+)	241-L6	244-A3/C2/ F2/J1	Gate contents of Y-register to Z-register
CLLTR-	241-L10	CPU	TL1	R	(H0LDM-)(TL1FF+) (MCRST+)	241-G10	242-C11/K11 and 243-C11/K11	Clears L-register
D1LAX	External device						241-A1/A2/ A3/A4	DMA cycle request lines from external device to DMA PN
STCHS+	241-J6	CPU	TL2	S	(TL2FF+)(MCSET+)	241-G6	241-A3	Set PN channel select flip-flops associated with active D1LAX lines
CHSLX-	241-C2/ C3/C4				PN channel select flip-flop set	241-G6	241-B2/B3/ B4	Enables setting of associated channel enable flip-flop (CHENX)
							251-H1/K1 253-H1/K1 255-H1/K1	Gate ACXXX lines to ACTXX lines
							257-B3/ D3/F3	Enables associated end of range signal ERCH-
							External device	Enables external device to gate data onto L1BXX lines
DMARQ+	241-C4				PN channel select flip-flop set	241-B2/ B3/B4	240-D11	Enables setting of TLAFF flip-flop thus enabling the starting of DMA timing level generator
							241-J7	Disables FZYTL+
DMARQ-	241-C4				PN channel select flip-flop set	241-B2/ B3/B4	241-F2	Generates DMCYQ-
DMACY+	241-L7				(TLAFF+)	241-L7	118-E5 240-H3 241-F2	Holds TL4FF reset Enables SAM1N-A Generates DMCYQ-
SETTA-	240-G11	CPU	TL3	S	(DMARQ+)(TL23F-)(TL24F+) (TACFF-)(TBCFF-) (MCSET-)	240-D10	118-G6	Resets TL3FF flip-flop
MEMC1+	126-J11	DMA	TLA	L	(TLAFF-)	126-J11	150-C1	Start memory cycle
MEMC1+B	149-J10	DMA	TLA	L	(TLAFF-)	149-J10	142-G10	Start memory cycle
DMAWR+	241-G8	DMA	TLA	L	(DMA1N+)(TLAFF+)	241-E7	126-G10	Causes write cycle (disables RRCXX)
CLYTR-	129-J3	DMA	TLA	R	(TLAFF+)(MCRST+)	129-F3/ H3	101---116-L11	Clears Y-register
EDMAY+	241-L3/L4	DMA	TLA	S	(TLAFF+)(MCSFT+)	241-G3/ J3	101---116-F10	Gates ACTXX lines to Y-register
ERCHX-	257-B3/ D3/F3	DMA	TLAB	L	(CHSLX+)(RCX01+ through RCX16+)(TLABF+)	257-A/ D/F	External device	End of range signal. Disables external device D1LAX+ signal
DMCYQ-	241-G2				(DMARQ+) (DMACY+)	241-F2	118-F5	Inhibits TL4FF

DMA Cycle Analysis (Cont)

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
SAMIN+	240-H3	DMA	TAC	S	(TACFF+)(TBDFF-)(MCSET-)	240-D9	240-D2 242/243-B3/G3	Enables setting of TLEFF flip-flop. Inhibits MMXXE lines (contents of accessed memory location) from M-register
TR1GX-	250-D1/D2/D3	DMA	TLB	L	(CHSLX+)(TLBFF+)	250-D1/D2/D3	251-F1, 253-F1, 255-F1	Increments contents of associated Address Counter by one
CLLTR-	241-L10	DMA	TLB	R	(TLBFF+)(MCRST+)	241-J10/L10	242-C11/K11 and 243-C11/K11	Clears L-register
1NSTR+	241-L2	DMA	TLB	S	(TLBFF+)(MCSET+)	241-J2	242-A1/G1 and 243-A1/G1	Strobes contents of L1BXX lines into L-register
STCHN+	241-L1	DMA	TLB	S	(TLBFF+)(MCSET+)	241-J2	241-A7/A9/C7/C9	Sets selected CHENX flip-flop and resets non-selected CHENX flip-flop
CHENX+	241-A7/A9/C7/C9				(CHSLX+)(STCHN+)	241-A7/A9/C7/C9	252, 254, 256-F10 External device	Enables TRRCX-. Enables external device to receive data from L0BXX lines
STCHS+	241-J6	DMA	TLC	S	(TLCFF+)(MCSET+)	241-G5	241-A3	Sets PN channel select flip-flops whose D1LAX lines are active. A set PN flip-flop generates CHSLX-, DMARQ+, and holds DMACY set to cause another DMA cycle immediately following the present DMA cycle
CLCHS-	241-J5	DMA	TLC	R	(TLCFF+)(MCRST+)	241-J5	241-A4	Resets PN channel select flip-flops whose D1LAX lines are not active. If all PN flip-flops are reset, CHSLX- and DMARQ are disabled and the resetting of DMACY is enabled
DMARQ-	241-C5				(D1LA1-)(D1LA2-)(D1LA3-)(D1LA4-)(CLCHS)	241-A2/A3/A4	240-D1/241-J7	Disables TLAFF flip-flop. Generates EZYTL+
EZYTL+	241-J7				(DMARQ-)	241-J7	244-B2/D1/H2/J1	Gates contents of Z-register to ACTXX lines
TRRCX-	252, 254, 256-F10	DMA	TLD	L	(CHENX+)(TLDFF+)	252, 254, 256-F10	252, 254, 256-F1	Increment range counter by one
DMAWR-	241-G9	DMA	TLD	S	(TLDFF+)(MCSET+)	241-E9	126-G10	Enables RRCXX

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
0TPMA-	240-H7	DMA	TLE	L	(TLEFF+)	240-H7	External device	Enables device to transfer contents of L0BXX lines into its buffer register
CLYTR-	129-J3	DMA	TLE	R	(TLEFF+)(MCRST+)	129-E3/ H3	101---116- L11	Clears Y-register
DMACY-	241-L8	DMA	TLE	R	(TLAEE-)(TLEFE+) (MCRST+)	241-J8	118-E5 240-H3	Enables TL4FF flip-flop. Resets SAMIN flip-flop
EDMAY+	241- L3/ L4	DMA	TLE	S	(TLEFF+)(MCSET+)	241-G3/ J3	101---116- F10	Gates ACTXX lines to Y-register
SAMIN-	240-H4				(DMACY-)	240-H3	242/243- B3/G3	Enables MMXXE lines to M-register

PARTS LIST

Table 1 contains the parts list for the items located in both the main frame and option drawer.

The A1 prefix reference designation is permanently assigned to the main frame and will not be reassigned. The XX prefix reference designation is for reference only and will be reassigned accordingly to each option drawer of a system's configuration.

Component parts for the μ-PAC Digital Modules, unless otherwise indicated, will be found on the data sheets included in 3C Doc. No. 130071620, Instruction Manual, DDP-516 General Purpose Computer, Vol. I, Theory of Operation and Maintenance.

LOGIC BLOCK DIAGRAMS

The logic block diagrams for the DDP-516-21 Direct Memory Access Option follow the parts list.

Refer to Table 2 for a list of signal mnemonics.

Table 1.
DDP-516-21 DMA Option Parts List

Reference Designation	Description	3C Part No.	Quantity Required
	The following items are located in the Main Frame logic drawer, A1-Unit, and are required for all DMA configurations.		
A1D11	μ-PAC DIGITAL MODULE--priority	Model CC-044	1
A1D12,13	μ-PAC DIGITAL MODULE--NAND power amplifier type II	Model CC-073	2
A1D14 A1F41,42,44, 45,46,47 A1F56 A1F63,64,65, 67,68	μ-PAC DIGITAL MODULE--NAND power amplifier type I	Model CC-045	13
A1E18, A1D18	μ-PAC DIGITAL MODULE--termination PAC	Model CC-154	2
A1D15 A1E11,12 A1F12,13,14, 15,16	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	8
A1D16,17 A1D33	μ-PAC DIGITAL MODULE--NAND gate type I	Model DI-335	3
A1D56	μ-PAC DIGITAL MODULE--parallel transfer gate	Model CM-022	1
A1E13,14,15, 17 A1F17	μ-PAC DIGITAL MODULE--power inverter	Model PA-336	5
A1E16	μ-PAC DIGITAL MODULE--gated flip-flop	Model CC-089	1

Table 1. (Cont)
DDP-516-21 DMA Option Parts List

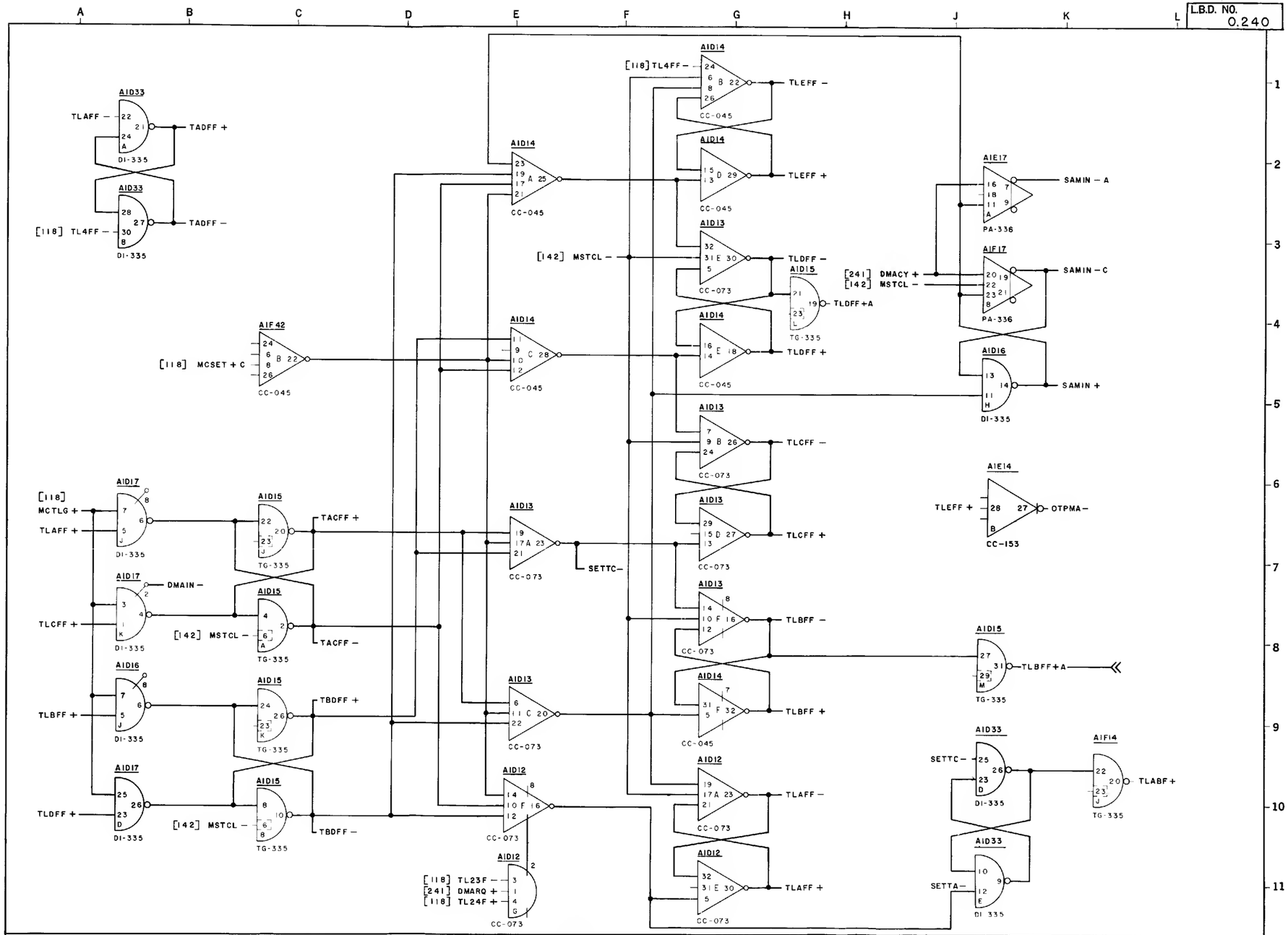
Reference Designation	Description	3C Part No.	Total Qty Req. for Channels:		
			1	2	3
	The following items are located in an option drawer; reference designations applicable to each channel are indicated as follows: 1st Channel --- No marking 2nd Channel --- Marked* 3rd Channel --- Marked #				
XXA11#,12#, 13#,14# XXB12*,13* XXB26,27 XXC12*,13* XXC26,27	μ-PAC DIGITAL MODULE--fast carry counter	Model CC-091	4	8	12
XXA15# XXB15* XXB23 XXC14*,23	μ-PAC DIGITAL MODULE--transfer gate PAC	Model CC-152	3	4	5
XXA17	μ-PAC DIGITAL MODULE--parallel transfer gate	Model CM-022	-	-	1
XXA16# XXB14*,17#,18 XXB22,24,25 XXC16*,17*,18 XXC22,25	μ-PAC DIGITAL MODULE--transfer gate	Model TG-335	7	10	12
XXA18# XXA22,23*	μ-PAC DIGITAL MODULE--multi-input NAND gate	Model DC-335	1	2	3
XXB16# XXC15* XXC24	μ-PAC DIGITAL MODULE--power inverter	Model PA-336	1	2	3
XXB21	μ-PAC DIGITAL MODULE--octal/decimal decoder	Model OD-335	1	1	1
XXA25	μ-PAC DIGITAL MODULE--NAND gate Type II	Model DL-335	1	1	1
XXA24	μ-PAC DIGITAL MODULE--gated flip-flop	Model CC-089	1	1	1
XXA/B/C1 XXA/B/C2	CONNECTOR PLANE ASSY--c/o 2 x 3 module (6 blocks of 8 connectors each), framework and associated parts; factory repairable only		1	1	1
	CABLE ASSY--interconnecting cable assemblies will be specified by each system configuration		AR	AR	AR

Table 2.
Function Index

Mnemonic	LBD/Grid	Description
OTPAX	250-B8	Output address pulse. Gates starting address on OTBXX to address counter.
OTPMA	240-H7	Output pulse used to strobe LOB into external device buffer register.
OTPRX	250-B9	Output range pulse. Gates two's complement of number of transfers on OTBXX lines to range counter.
INSTR	241-L2	Input strobe. Gates LIBXX lines to L-register.
ACXXX	251-J/L 253-J/L 255-J/L	Address counter output lines.
ACKAX	241-C3	Acknowledge DILAX lines.
ACTXX	244, 251, 253, 255	Address count transfer lines 1 through 16 from Z register or address counter to Y-register.
ADQ24	250-G11	Address ;equals 24 control signals.
CHENX	241-A8/C8	Channel enable flip-flops. Enables output bus lines (LOBXX) to external device.
CHSLX	241-C3	Channel select signal used to set associated channel enable (CHENX) flip-flop. Also enables external device to gate data onto the input bus lines LIBXX.
CLCHS		Clear channel select flip-flops (in priority network).
CLLTR	241-L10	Clear L-register signal.
CLZTL	241-L5	Clear Z-register signal.
DILAX	241-A3	Data interrupt lines from external device to request DMA cycle.
DMACY	241-L7	DMA cycle control signal.
DMARQ	241-C5	DMA cycle request signal. Occurs when an active request (DILAX) has been sampled.
DMAWR	241-G8	DMA write/read control flip-flop.
DMCYQ	241-G2	DMA cycle request signal for main frame.
EDMAY	241-L3	Enable DMA address counter lines to Y-register.
ERCHX		End of range signal to external device.
ERLAX		End of range signal for "INA" instruction.
EYZTL	241-L6	Enable Y-register to Z-register transfer signal.

Table 2. (Cont)
Function Index

Mnemonic	LBD/Grid	Description
EZYTL	241-J7	Enable Z-register to Y-register transfer signal.
LIBXX	242-243	L-register input bus lines. Data from external device.
LXXFF	242-243	L-register flip-flops.
MMXXE	242-243	Memory output lines to M-register.
RCXXX	252-G 254-G 256-G	Range counter output lines.
SAXXX	251-C/D 253-C/D 255-C/D	Set address counter lines.
SAMIN	240-H3	Sense amplifier to M-register inhibit signal.
SETTA	240-G11	Set TLAFF flip-flop signal.
SRXXX	252-B/D 254-B/D 256-B/D	Set range counter lines.
STCHN	241-L1	Set channel enable flip-flop.
STCHS	241-J6	Set channel select flip-flop (priority network flip-flop).
TACFF	240-C6	Timing level A through timing level C flip-flop.
TADFF	240-A2	Timing level A through timing level D flip-flop.
TBDFF	240-C9	Timing level B through timing level D flip-flop.
TLAFF	240-G10	Timing level A flip-flop (first DMA timing level).
TLBFF	240-G9	Timing level B flip-flop (second DMA timing level).
TLCFF	240-G7	Timing level C flip-flop (third DMA timing level).
TLDFF	240-G4	Timing level D flip-flop (fourth DMA timing level).
TLEFF	240-G2	Timing level E flip-flop (fifth DMA timing level). When set, remains set until CPU timing level TL4 is generated.
TRIGX	250-D2	Increments address counter contents by one.
TRRCX	252, 254 256-F10	Increments range counter by one.
ZXXFF	244	Z-register flip-flops.


L.B.D. NO. 0.240
A1D33
TLAFF –
TADFF +
DI-335
TADFF –
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A1D14
[118] TL4FF –
TLEFF –
CC-045
TLEFF +
A1D13
[142] MSTCL –
TLDFF –
CC-073
A1D15
TG-335
TLDFF +A
TLDFF +
A1F42
[118] MCSET + C
A1E17
SAMIN – A
PA-336
A1F17
SAMIN – C
[241] DMACY +
[142] MSTCL –
A1D16
SAMIN +
A1D17
[118] MCTLG +
TLAFF +
TACFF +
DMAIN –
TLCFF +
[142] MSTCL –
TACFF –
TBDFF +
TLBFF +
TBDFF –
TLDFF +
SETTC–
TLCFF –
TLCFF +
TLBFF –
TLBFF +
TLAFF –
TLAFF +
A1E14
TLEFF +
OTPMA–
CC-153
A1D15
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A1D33
SETTC–
A1F14
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[118] TL23F –
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[118] TL24F +
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HONEYWELL
INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass
DR. A. Kuytzer
DATE 1/17/67
ENG.
APP.
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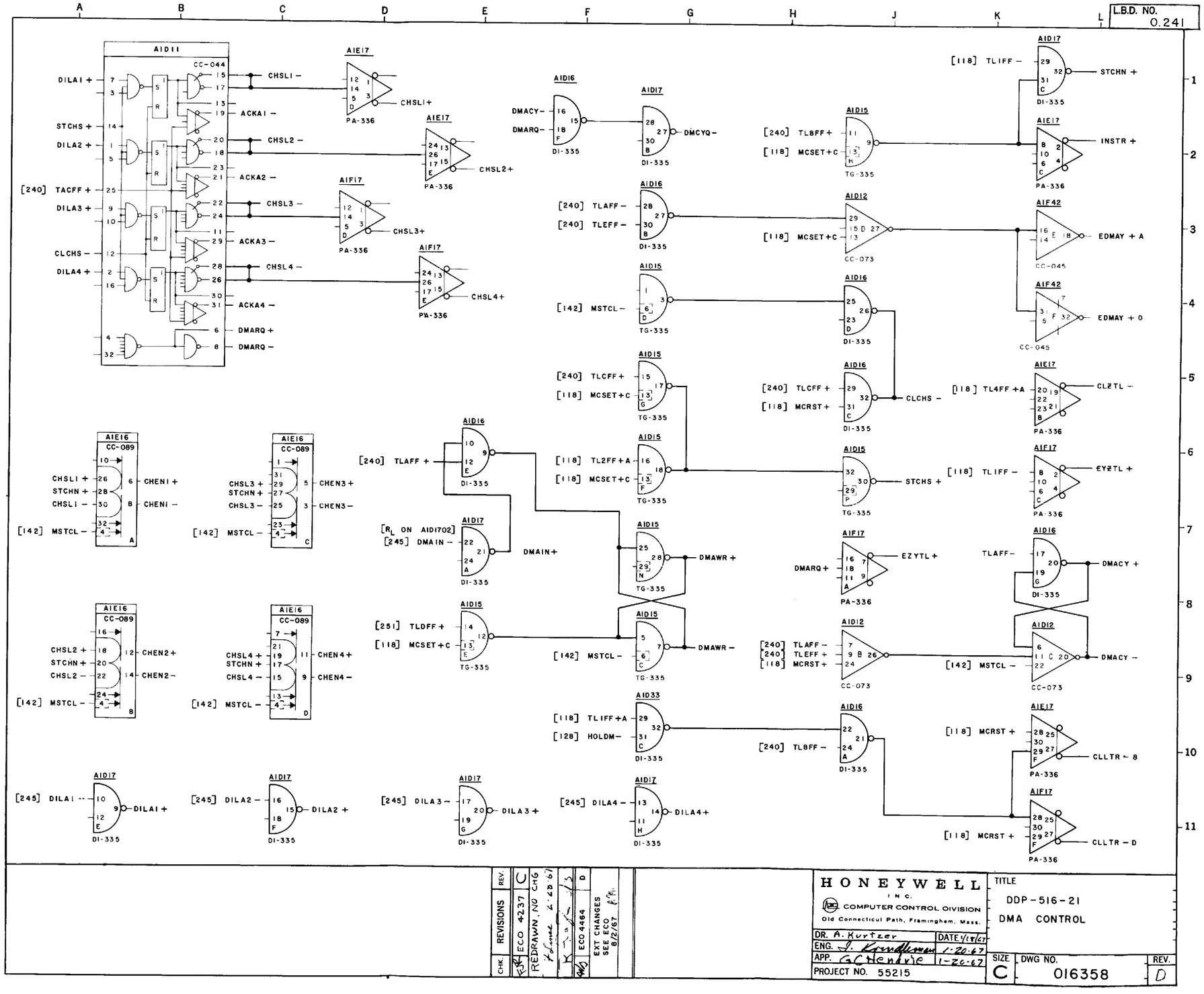
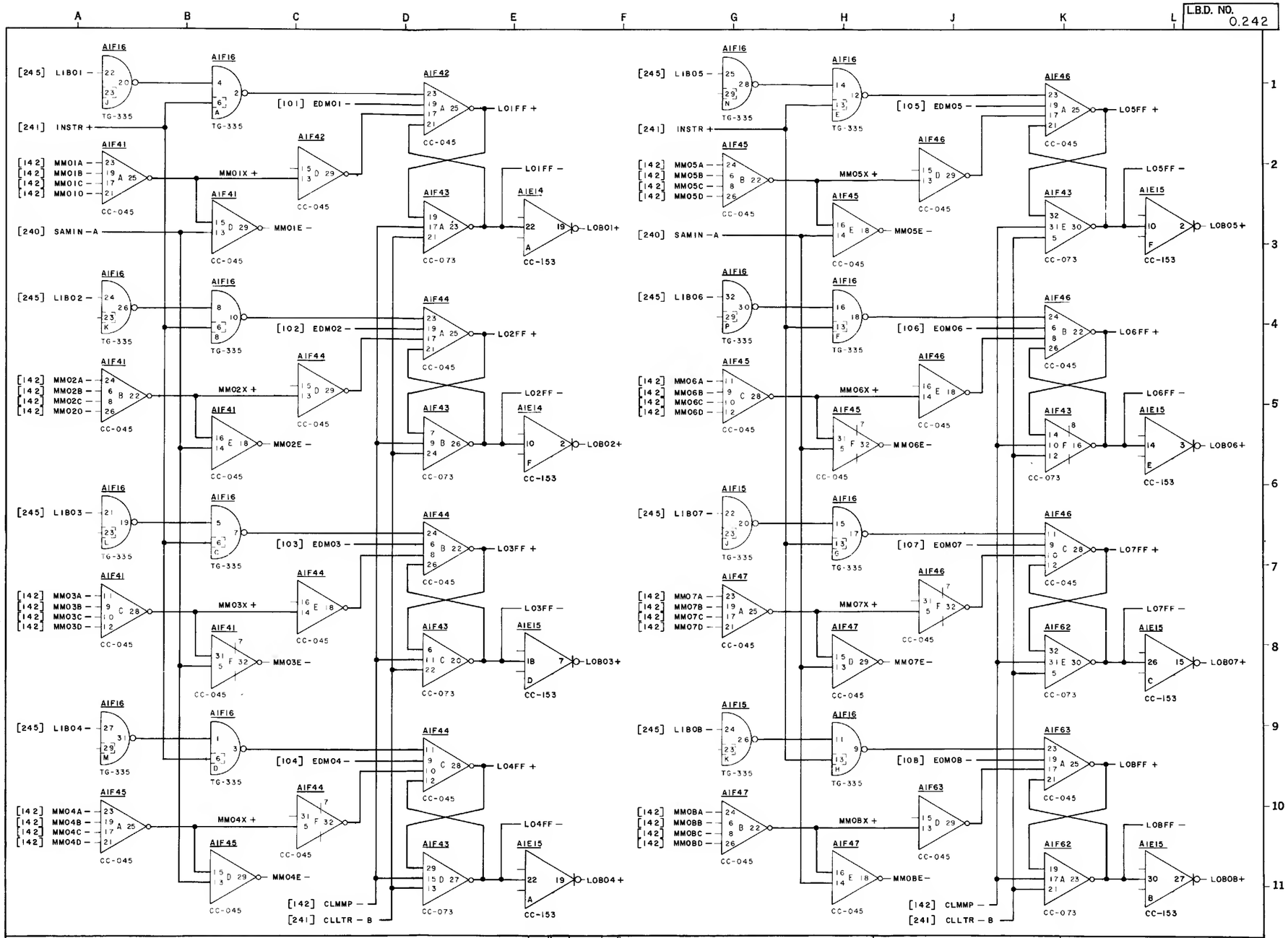
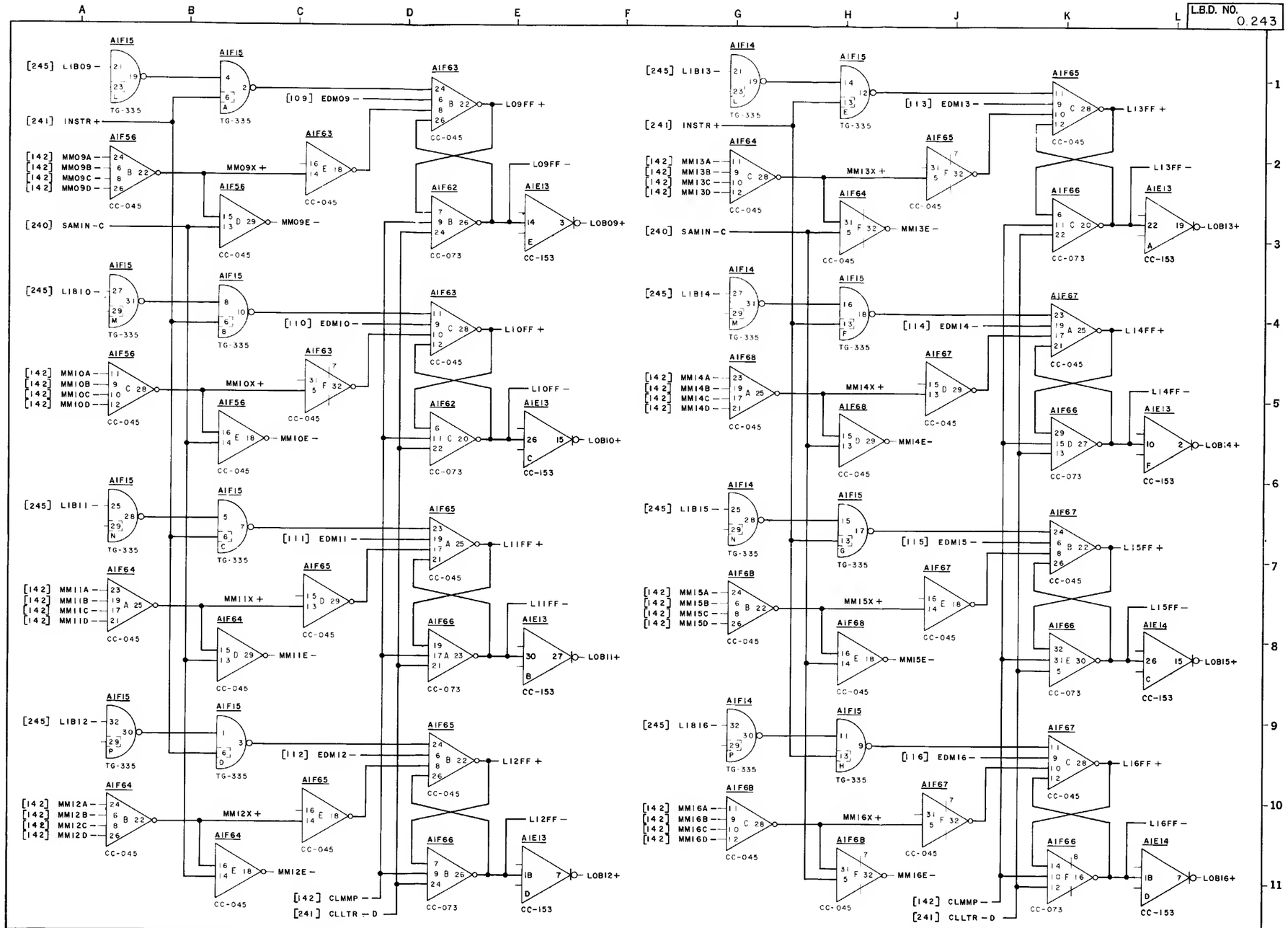
TITLE
DDP-516-21
DMA TIMING LEVEL GEN.
SIZE C
DWG NO. 016357
REV.


L.B.D. NO. 0.241
AID11
CC-044
DILA1 +
STCHS +
DILA2 +
[240] TACFF +
DILA3 +
CLCHS –
DILA4 +
CHSL1 –
ACKA1 –
CHSL2 –
ACKA2 –
CHSL3 –
ACKA3 –
CHSL4 –
ACKA4 –
DMARQ +
DMARQ –
AIE17
CHSL1+
CHSL2+
CHSL3+
CHSL4+
PA-336
AIF17
AID16
DMACY–
DMARQ–
DI-335
AID17
DMCYQ–
[118] TL1FF –
STCHN +
INSTR +
AID15
[240] TL8FF +
[118] MCSET+C
TG-335
[240] TLAFF –
[240] TLEFF –
AID12
CC-073
[118] MCSET+C
AIF42
EDMAY + A
CC-045
EDMAY + 0
[142] MSTCL –
[240] TLCFF +
[118] MCSET+C
[118] MCRST +
CLCHS –
[118] TL4FF +A
CLZTL –
[118] TL2FF+A
STCHS +
[118] TL1FF –
EYZTL +
AIE16
CC-089
CHSL1 +
STCHN +
CHSL1 –
CHENI +
CHENI –
[142] MSTCL –
CHSL3 +
STCHN +
CHSL3 –
CHEN3+
CHEN3–
[240] TLAFF +
[R_L ON AID1702]
[245] DMAIN –
DMAIN+
DMAWR +
DMAWR –
EZYTL +
DMARQ +
TLAFF –
DMACY +
DMACY –
[251] TLDFF +
[118] MCSET+C
[142] MSTCL –
[240] TLAFF –
[240] TLEFF +
[118] MCRST +
CHSL2 +
STCHN +
CHSL2 –
CHEN2+
CHEN2–
CHSL4 +
STCHN +
CHSL4 –
CHEN4+
CHEN4–
AID33
[118] TL1FF+A
[128] HOLDM–
[240] TL8FF –
[118] MCRST +
CLLTR – 8
CLLTR – D
[245] DILA1 –
DILA1 +
[245] DILA2 –
DILA2 +
[245] DILA3 –
DILA3 +
[245] DILA4 –
DILA4 +
REVISIONS
REV.
CHK.
ECO 4237
REDRAWN, NO CHG
ECO 4464
EXT CHANGES SEE ECO 8/2/67
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. A. Kurtzer
ENG. J. Kandelman 1-20-67
APP. G.C. Henryle 1-26-67
PROJECT NO. 55215
TITLE
DDP-516-21
DMA CONTROL
SIZE C
DWG NO. 016358
REV. D


L.B.D. NO. 0.242
[245] LIB01 –
[241] INSTR +
[142] MM01A –
[142] MM01B –
[142] MM01C –
[142] MM01D –
[240] SAMIN – A
[101] EDM01 –
MM01X +
MM01E –
L01FF +
L01FF –
L0B01+
[245] LIB02 –
[102] EDM02 –
MM02X +
MM02E –
L02FF +
L02FF –
L0B02+
[245] LIB03 –
[103] EDM03 –
MM03X +
MM03E –
L03FF +
L03FF –
L0B03+
[245] LIB04 –
[104] EDM04 –
MM04X +
MM04E –
L04FF +
L04FF –
L0B04+
[142] CLMMP –
[241] CLLTR – B
[245] LIB05 –
[105] EDM05 –
MM05X +
MM05E –
L05FF +
L05FF –
L0B05+
[245] LIB06 –
[106] EOM06 –
MM06X +
MM06E –
L06FF +
L06FF –
L0B06+
[245] LIB07 –
[107] EOM07 –
MM07X +
MM07E –
L07FF +
L07FF –
L0B07+
[245] LIB0B –
[10B] EOM0B –
MM0BX +
MM0BE –
L0BFF +
L0BFF –
L0B0B+
[142] CLMMP –
[241] CLLTR – B
AIF16
AIF41
AIF42
AIF43
AIF44
AIF45
AIF46
AIF47
AIF15
AIF62
AIF63
AIE14
AIE15
TG-335
CC-045
CC-073
CC-153
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.
DR. A. Kurtzev
ENG.
APP.
PROJECT NO. 55215
DATE 11/4/67
TITLE
DDP – 516 – 21
L REGISTER
BITS 1 – 8
SIZE C
DWG NO. 016359
REV.
REVISIONS
REV.
CHK.
ECO 4237
REDRAWN, NO CHG

L.B.D. NO. 0.243



REV.	REVISIONS	CHK
C	ECO 4237 REDRAWN, NO CHG 2-28-67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kuytzer	DATE 1/18/67
ENG.	/ / 67
APP.	/ / 67
PROJECT NO. 55215	

TITLE
DDP-516-21
L REGISTER
BITS 9-16

SIZE C | DWG NO. 016360 | REV.

L.B.D. NO. 0.244

[101] Y01FF –
EYŻTL + [241]
[241] CLŻTL –
[102] Y02FF –
[103] Y03FF –A
[104] Y04FF –A
[105] Y05FF –A
EYŻTL + [241]
[241] CLŻTL –
[106] Y06FF –A
[107] Y07FF –A
[108] Y08FF –A
[109] Y09FF –A
EYŻTL + [241]
[241] CLŻTL –
[110] Y10FF –A
[111] Y11FF –A
[112] Y12FF –A
[113] Y13FF –A
EYŻTL + [241]
[241] CLŻTL –
[114] Y14FF –A
[115] Y15FF –A
[116] Y16FF –A

[241] EŻYTL +

A1F14 / A1E11 / A1E12 / A1F13 / A1F12 — TG-335

ACT01 +
ACT02 +
ACT03 +
ACT04 +
ACT05 +
ACT06 +
ACT07 +
ACT08 +
ACT09 +
ACT10 +
ACT11 +
ACT12 +
ACT13 +
ACT14 +
ACT15 +
ACT16 +

Ż01FF – / Ż01FF +
Ż02FF – / Ż02FF +
Ż03FF – / Ż03FF +
Ż04FF – / Ż04FF +
Ż05FF – / Ż05FF +
Ż06FF – / Ż06FF +
Ż07FF – / Ż07FF +
Ż08FF – / Ż08FF +
Ż09FF – / Ż09FF +
Ż10FF – / Ż10FF +
Ż11FF – / Ż11FF +
Ż12FF – / Ż12FF +
Ż13FF – / Ż13FF +
Ż14FF – / Ż14FF +
Ż15FF – / Ż15FF +
Ż16FF – / Ż16FF +

NOTES:

REV.	REVISIONS	CHK.
B	ECO 4237	FJK
	REDRAWN NO CHG 2.28.67	

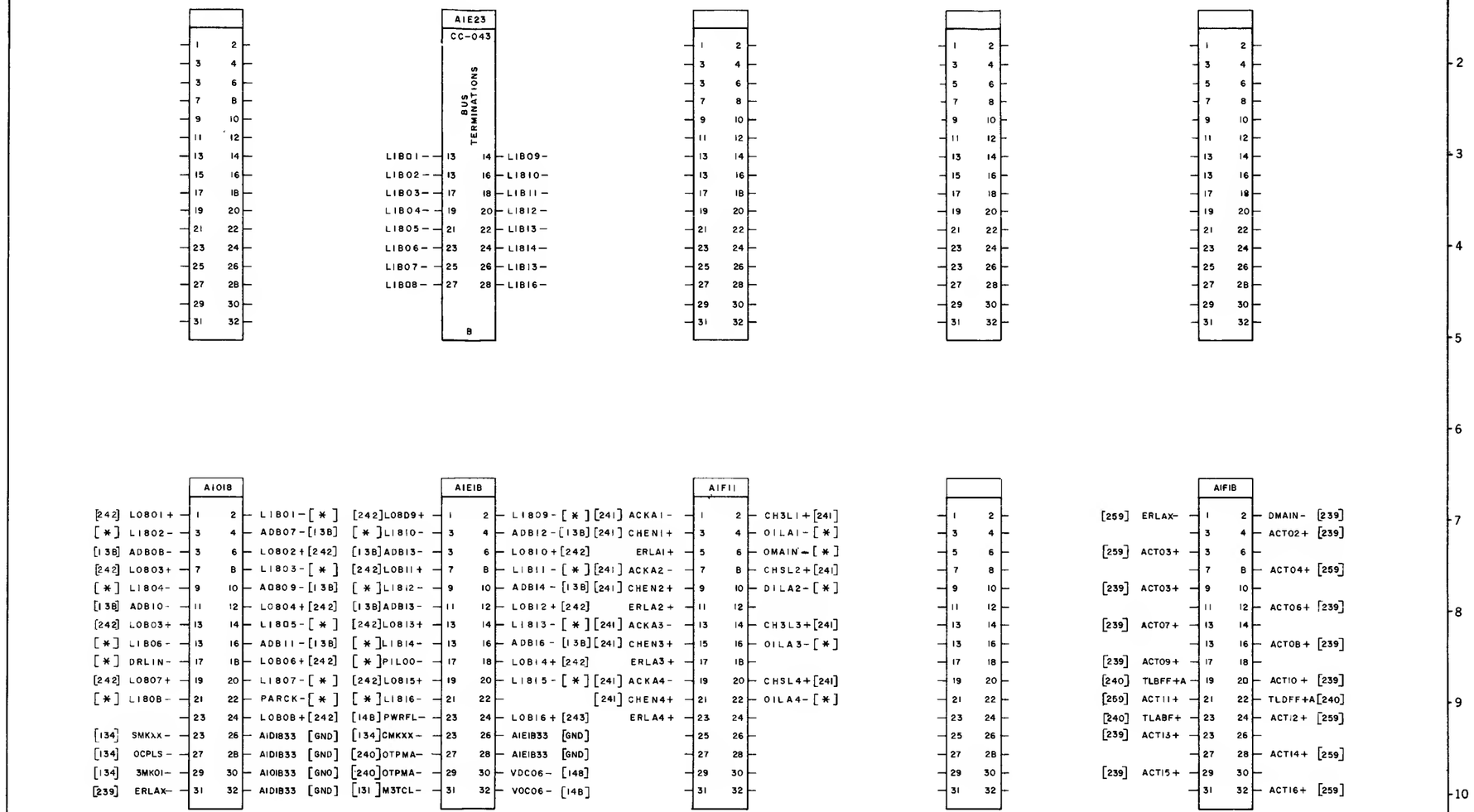
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/15/67
ENG.	
APP.	
PROJECT NO. 55215	

TITLE
DDP – 516 – 21
DMA Ż REGISTER

SIZE C | DWG NO. 016361 | REV. B

L.B.D. NO. 0.245



[*] THESE SIGNALS ARRIVE BY BUS FROM I/O OPTIONS, DEPENDING ON SYSTEM CONFIGURATION

REVISIONS

REV	
K	TAKEN FROM SR64-1394 DUCKWORTH 10/66
A	ECO 3767 1/23/67 JD
B	ECO 4131 MINOR CHG 11/11/67
C	

COMPUTER CONTROL COMPANY, INC
FRAMINGHAM MASS LOS ANGELES 64 CALIF

DR. A. Kurfzer	DATE 10/4/66
ENG	10-6-66
APP G C Hendyle	10-24-66
PROJECT NO. 55215	

TITLE
DCP-516-21
DMA CABLE
CONNECTORS

SIZE	DWG NO.	REV.
C	016362	C

L.B.D NO 0.248

HINGE

	F	E	D	C	B	A	
8	CC-045 ⚠1						6
7	CC-045						
6							
5	CC-045						
4	CC-045 ⚠1						
3	CC-045						
2							
1							
8							5
7							
6	CC-045 ⚠1		CM-022 ⚠1				
5							
4							
3							
2							
1							
8	CC-045 ⚠1						4
7	CC-045						
6	CC-045 ⚠1						
5	CC-045						
4							
3	CC-045						
2	CC-045 ⚠1						
1							
8							3
7							
6							
5							
4							
3			DI-335				
2							
1							
8							2
7							
6							
5							
4							
3							
2							
1							
8	CONN	CC-154 ⚠2	CC-154 ⚠2				1
7	PA-336	PA-336	DI-335				
6	TG-335	CC-089	DI-335				
5	TG-335	CC-153	TG-335				
4	TG-335	CC-163	CC-045				
3	TG-335	CC-153	CC-073				
2	TG-335	TG-335	CC-073				
1	CONN	TG-335	CC-044				

⚠1 THESE PACS ARE SHARED WITH THE EXTENDED ADDR OPTION

⚠2 CC-154 IN LOCATIONS E18 AND D18 SHOULD BE REMOVED AND PLACED IN LAST OPTION AT END OF OMA BUS WHEN OPTIONS ARE USED

REVISIONS

K	TAKEN FROM SK64-1394 DUCKWORTH 10-25-66
A	
B	ECO 3707 EXT CHANGES 1/23/67
C	ECO 3995 EXT CHANGES 2/20/67
D	ECO 4226 EXT CHANGES SEE ECO 5/25/67

COMPUTER CONTROL COMPANY, INC
FRAMINGHAM MASS LOS ANGELES 64 CALIF

DR. A. SVETZER	DATE 10-24-66
ENG.	10-24-66
APP. G.C. HENDRIE	10-24-66
PROJECT NO 55215	

TITLE
DMA
MF PAC ALLOCATION
DDP-516-21

SIZE C | DWG NO. 016586 | REV. D

L.B.D. NO. 0.249

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

4

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

3

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
6															
5															
4															
3															
2															
1															

	LOC	PAC	A	B	C	O	E	F	G	H	J	K	L	M	N	P
	8	CONN														
	7															
	6															
001	5	DL-335														
001	4	CC-089														
002	3	DC-335														
001	2	DC-335														
	1	CONN														

2

	LOC	PAC	A	B	C	O	E	F	G	H	J	K	L	M	N	P
	8	CONN														
001	7	CC-091														
001	6	CC-091														
001	5	TG-335														
001	4	TG-335														
001	3	CC-152														
001	2	TG-335														
001	1	OD-335														

	LOC	PAC	A	B	C	O	E	F	G	H	J	K	L	M	N	P
	8	CONN														
001	7	CC-091														
001	6	CC-091														
001	5	TG-335														
001	4	PA-336														
001	3	CC-152														
001	2	TG-335														
	1	CONN														

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
003	8	DC-335														
003	7	CM-022														
003	6	TG-335														
003	5	CC-152														
003	4	CC-091														
003	3	CC-091														
003	2	CC-091														
003	1	CC-091														

1

A

	LOC	PAC	A	B	C	O	E	F	G	H	J	K	L	M	N	P
001	8	TG-335														
003	7	TG-335														
003	6	PA-336														
002	5	CC-152														
002	4	TG-335														
002	3	CC-091														
002	2	CC-091														
	1	CONN														

B

	LOC	PAC	A	B	C	O	E	F	G	H	J	K	L	M	N	P
001	8	TG-335														
002	7	TG-335														
002	6	TG-335														
002	5	PA-336														
002	4	CC-152														
002	3	CC-091														
002	2	CC-091														
	1	CONN														

C

PAC SIDE

001 DMA WITH 1 CHANNEL
002 1st ADDITIONAL CHANNEL (CHANNEL 2)
003 2nd ADDITIONAL CHANNEL (CHANNEL 3)

REVISIONS

LTR	
A	TAKEN FROM SK64-1394 DUCKWORTH 10-25-66
B	ECO 4501
C	ECO 4042 EXT. CHANGES JD. 8/4/67

EXT. CHANGES SEE ECO

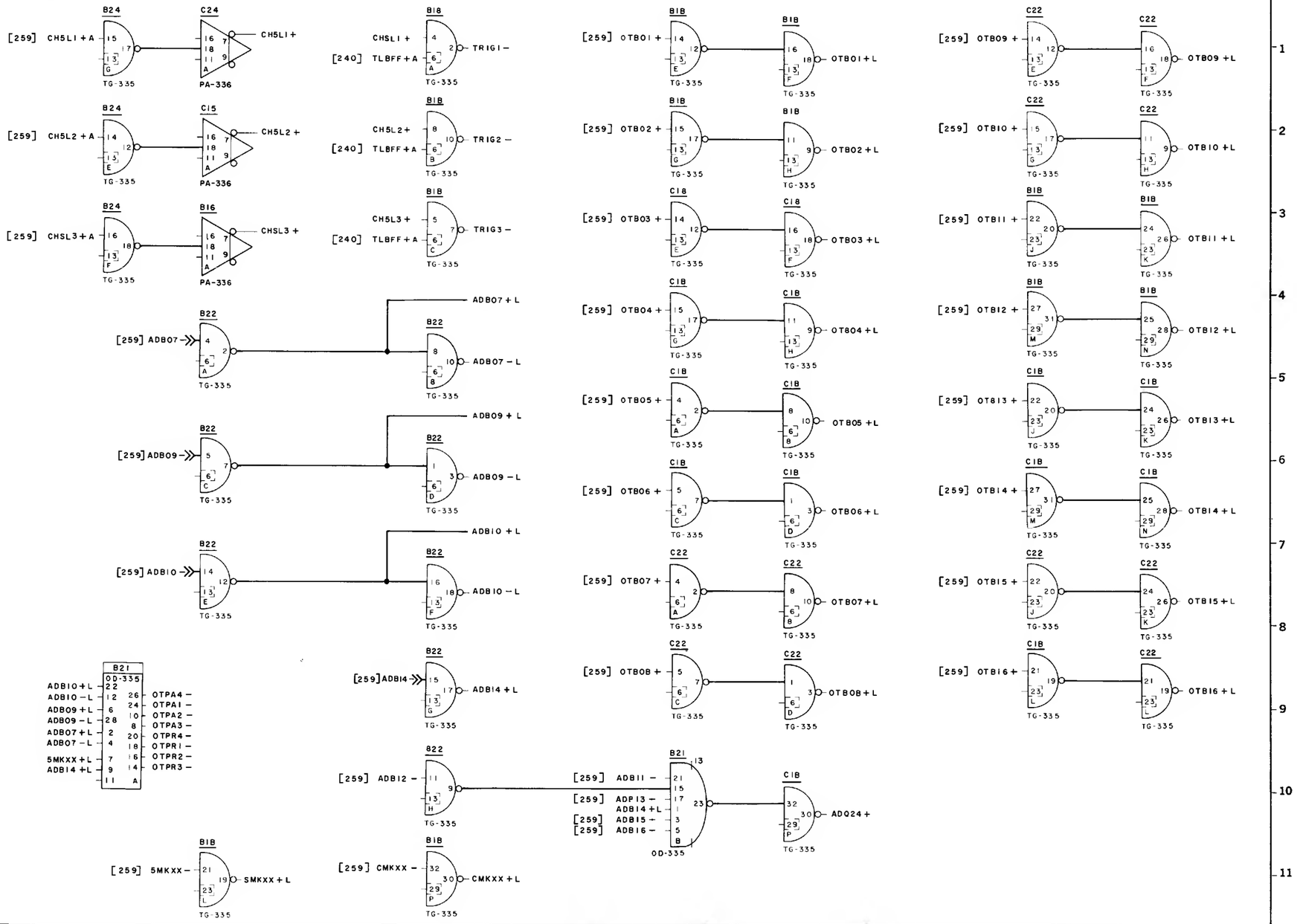
COMPUTER CONTROL COMPANY, INC
FRAMINGHAM MASS LOS ANGELES 64 CALIF

DR. A. KUETZER	DATE 10-24-66
ENG.	10-24-66
APP. R.C. Hendrie	10-24-66
PROJECT NO. 55215	

TITLE
DMA
2 X 3 PAC ALLOCATION
DDP-516-21

SIZE C | DWG NO. 016585 | REV. C

L.B.D. NO. 0.250



NOTES:

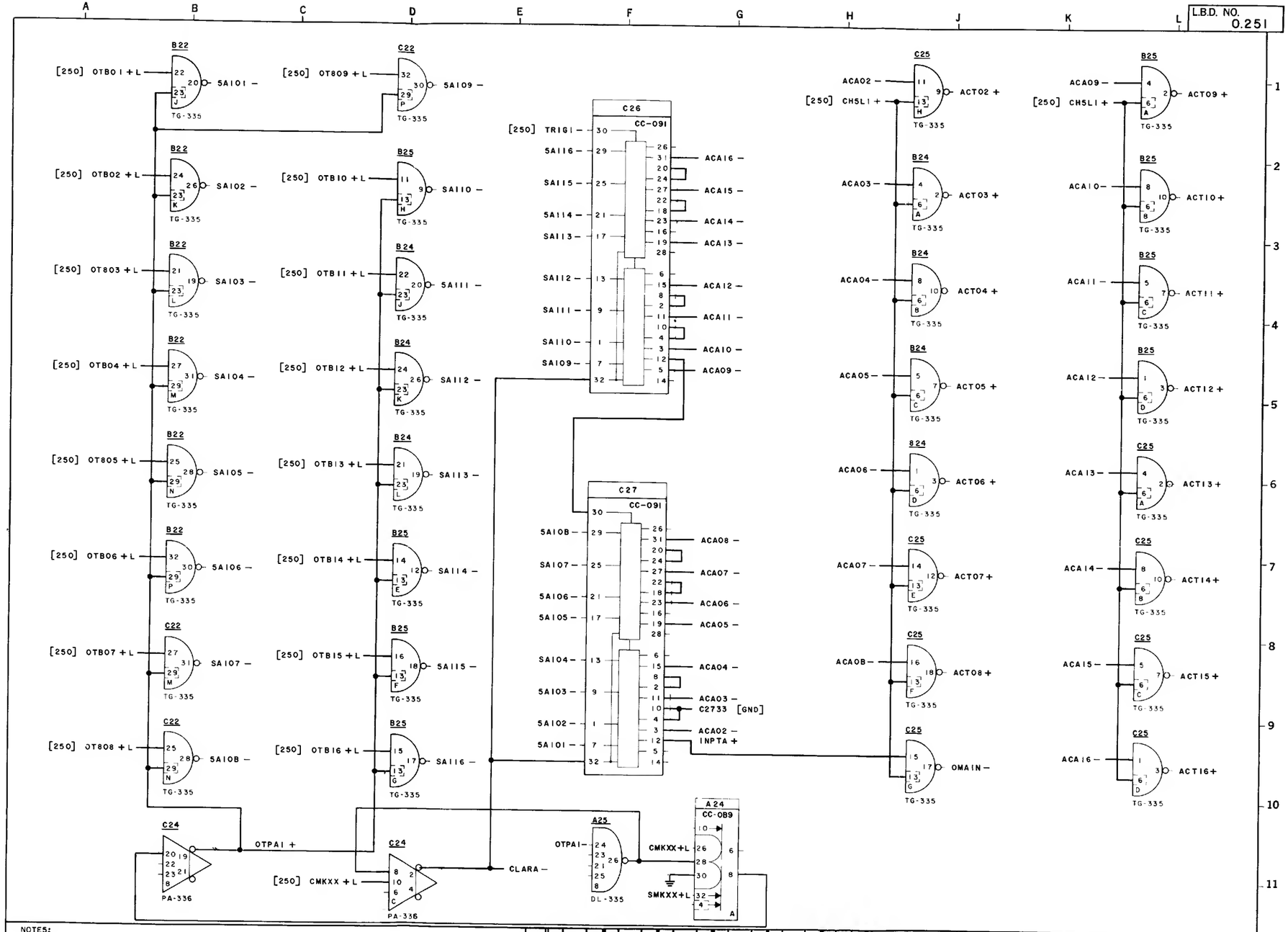
REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG 2-28-67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/18/67
ENG.	1-20-67
APP. G.C. Hendrie	1-26-67
PROJECT NO. 55215	

TITLE
DMA I/O BUS INTERFACE
DDP-516-21

SIZE	DWG NO.	REV.
C	016363	B



NOTES:

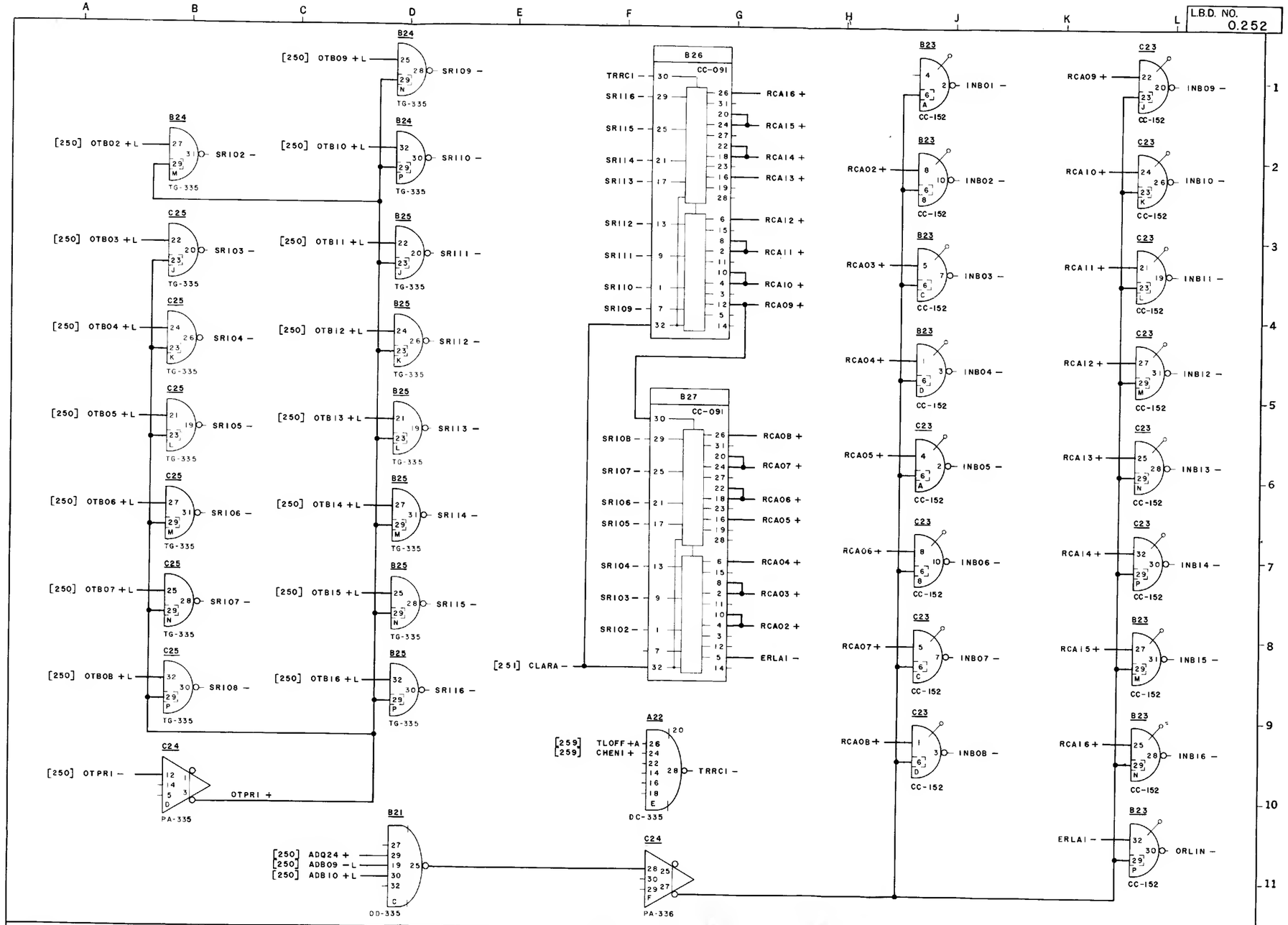
REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG 2-28-67	
C	ECO 4042 EXT. CHANGES J.D. 8/3/67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/13/67
ENG.	1-20-67
APP. G.C. Hendrie	1-20-67
PROJECT NO. 55215	

TITLE
DDP-516-21
DMA CHANNEL #1
ADDRESS COUNTER

SIZE C | DWG NO. 016364 | REV. C



NOTES:

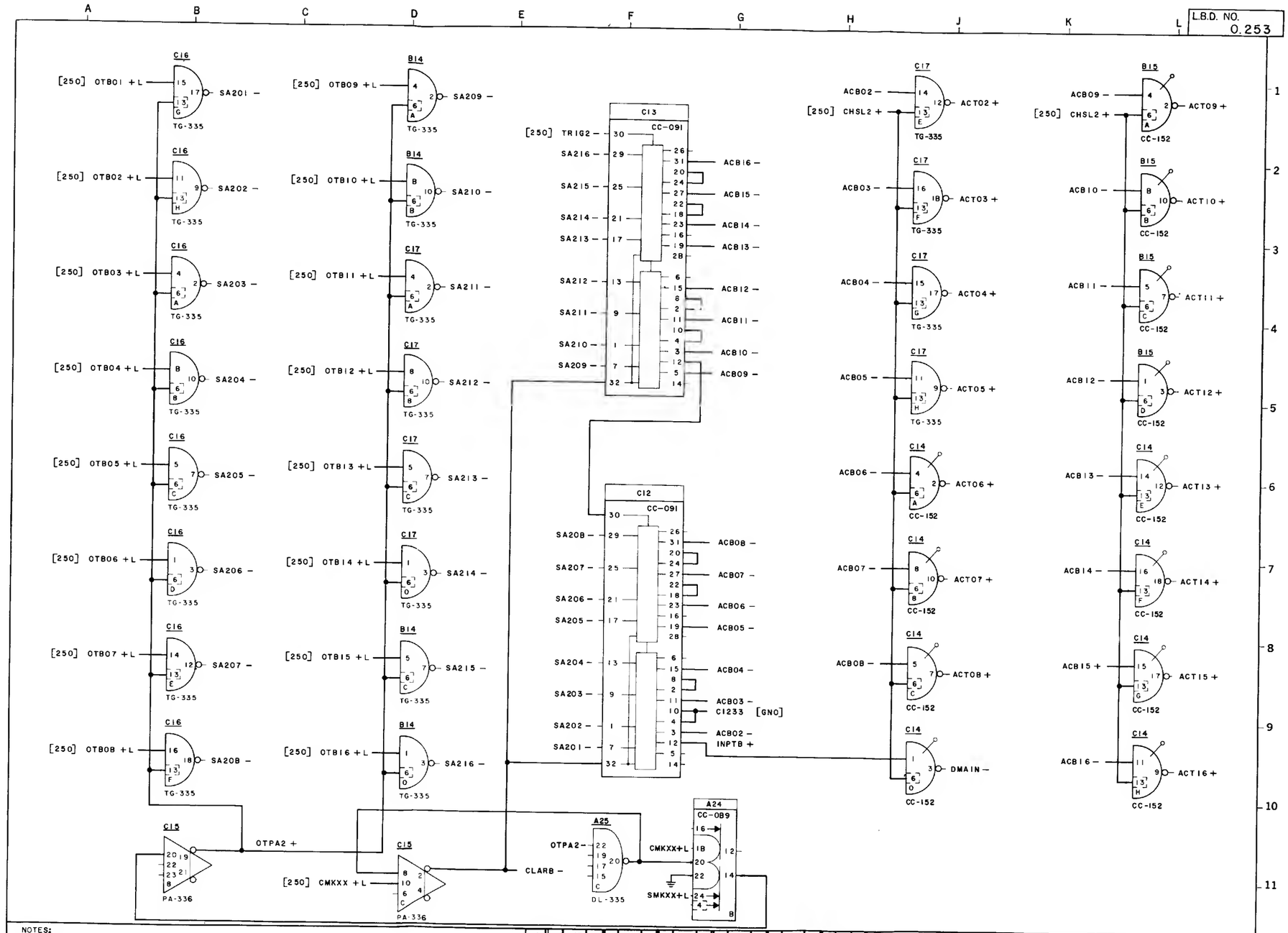
REVISIONS	REV.	CHK
ECO 4237 REDRAWN. NO CHG 2-28-67	B	
ECO 4042 EXT. CHANGES J.D. 8/3/67	C	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/18/67
ENG. W. Lyons	1-20-67
APP. G.C. Henderie	1-20-67
PROJECT NO. 55215	

TITLE
DDP-516-21
DMA CHANNEL #1
RANGE COUNTER

SIZE C | DWG NO. 016365 | REV. C



NOTES:

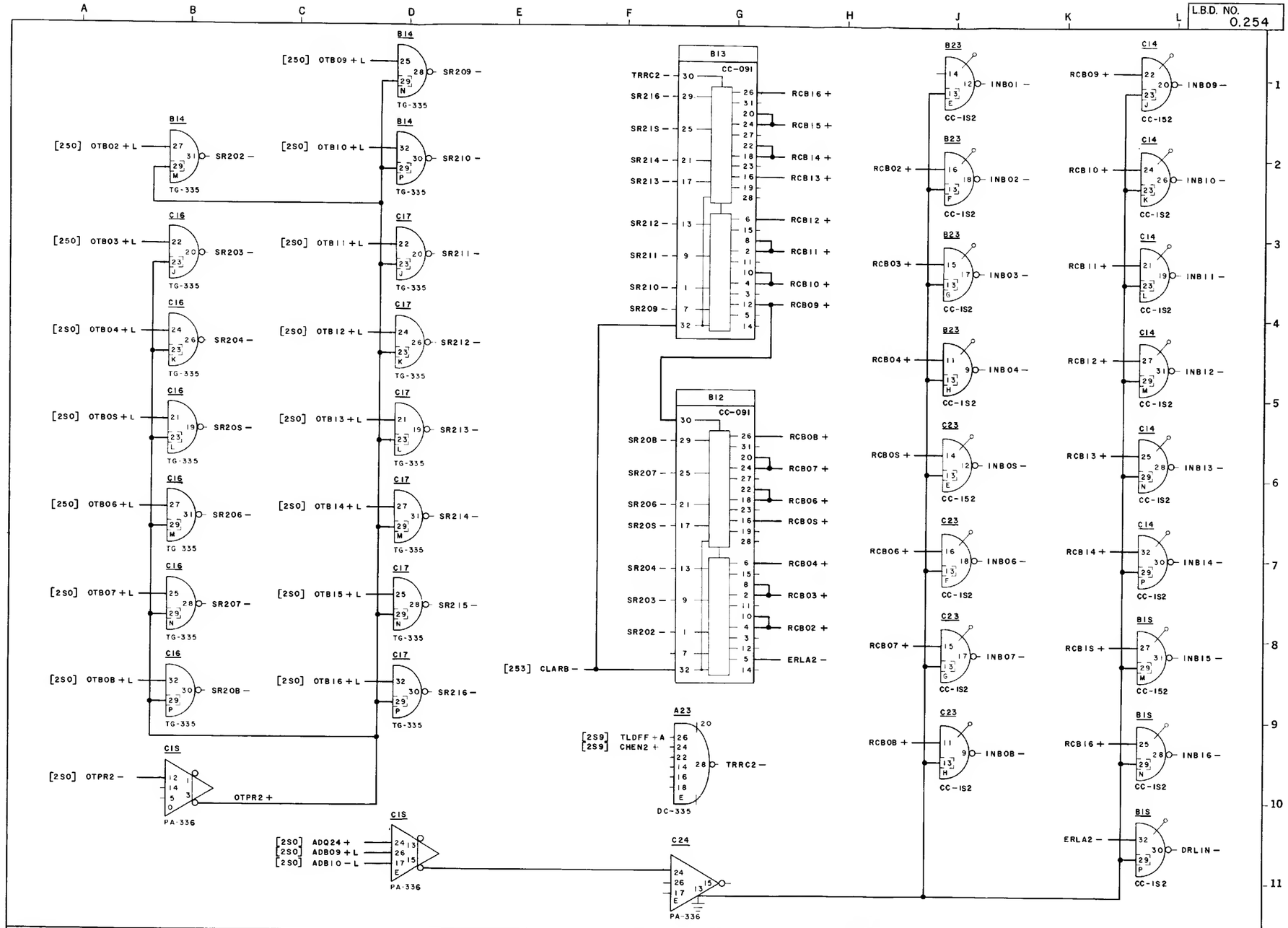
REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG 2-28-67	
C	ECO 4042 EXT. CHANGES JD 8/4/67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kyrtzer	DATE 1/19/67
ENG. J. W. Hayter	1-20-67
APP. G. C. Hendrie	1-24-67
PROJECT NO. 55215	

TITLE
DDP-516-21
DMA CHANNEL #2
ADDRESS COUNTER

SIZE C | DWG NO. 016366 | REV. C



NOTES:

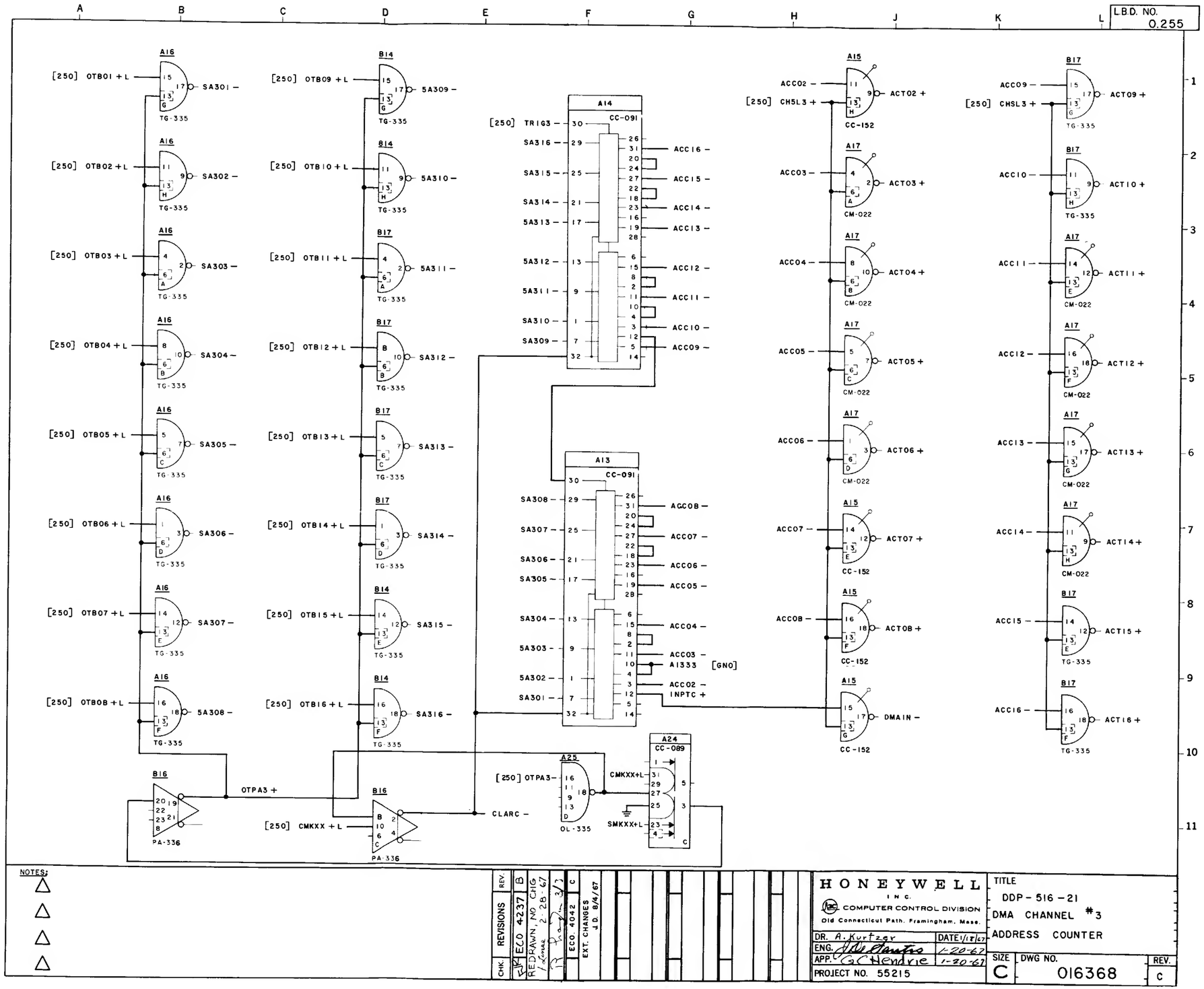
REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG Release 2-28-67	RJ
C	ECO 4042 EXT. CHANGES J.D. 8/4/67	

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kyrtzer	DATE 1/18/67
ENG.	1-20-67
APP.	1-20-67
PROJECT NO. 55215	

TITLE
DDP-516-21
DMA CHANNEL #2
RANGE COUNTER

SIZE C | DWG NO. 016367 | REV. C



NOTES:

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REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG 2-28-67	
C	ECO. 4042 EXT. CHANGES J.D. 8/4/67	

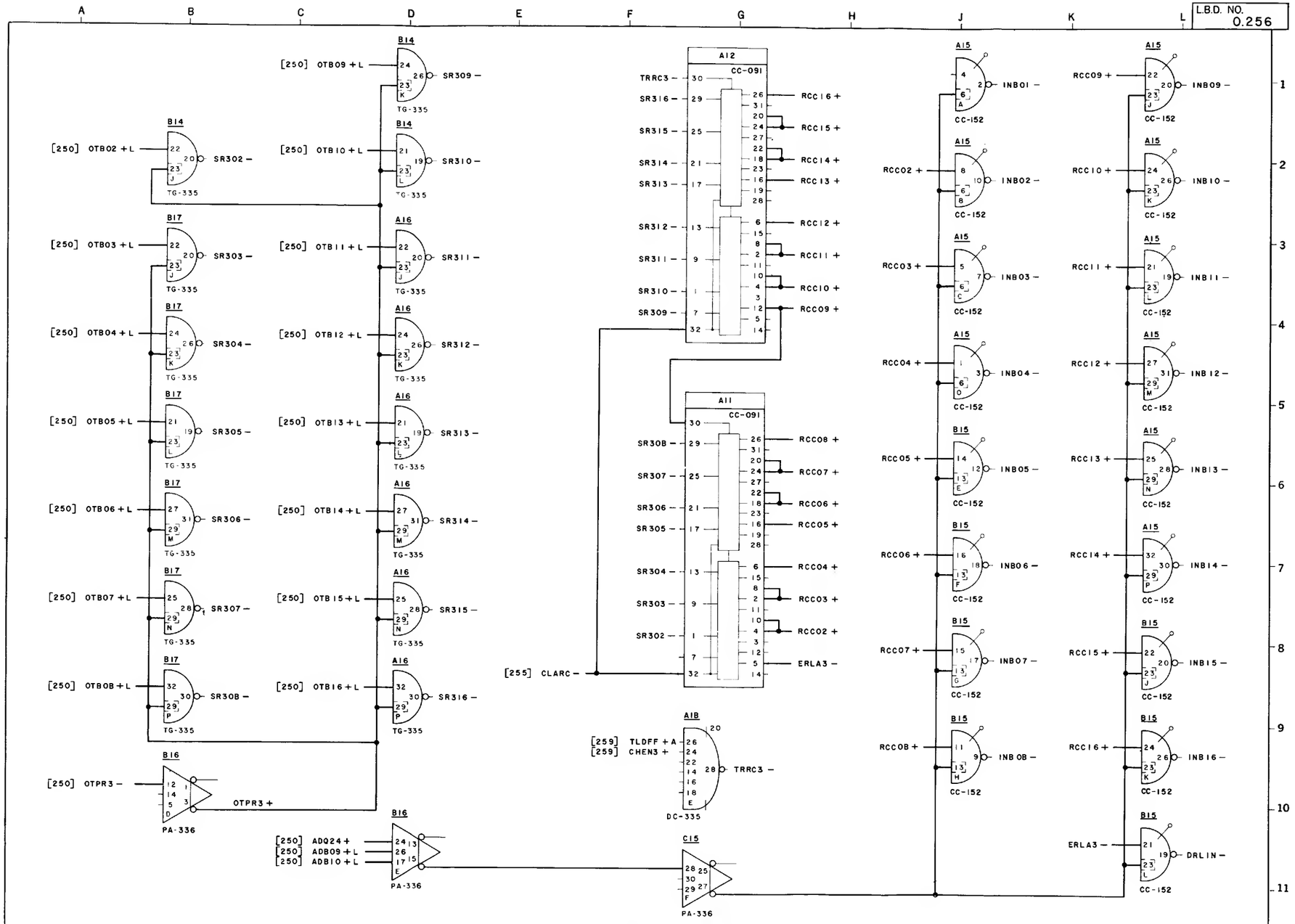
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/17/67	
ENG.	1-20-67	
APP.	1-20-67	
PROJECT NO. 55215		

TITLE
DDP-516-21
DMA CHANNEL #3
ADDRESS COUNTER

SIZE	DWG NO.	REV.
C	016368	C

L.B.D. NO. 0.256



NOTES:

REV.	REVISIONS	CHK.
B	ECO 4237 REDRAWN, NO CHG 2-28-67	
C	ECO 4042 EXT. CHANGES J.D. 8/4/67	

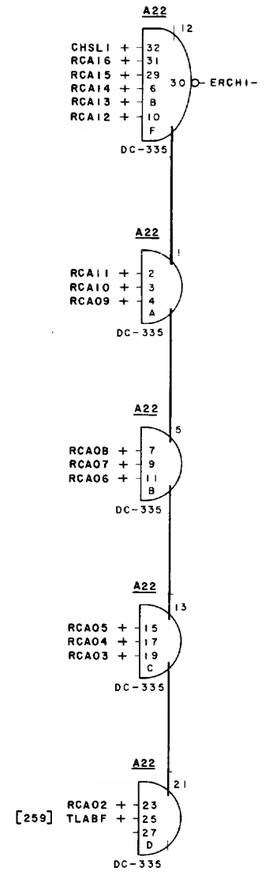
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

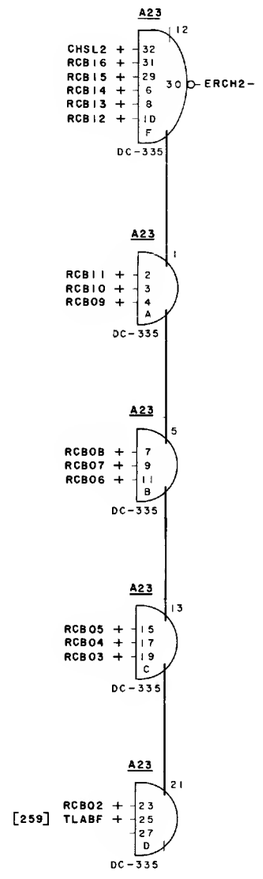
DR. A. Kurtzer	DATE 1/19/67
ENG. Eddie Hayden	1-20-67
APP. G C Hendrie	1-20-67
PROJECT NO. 55215	

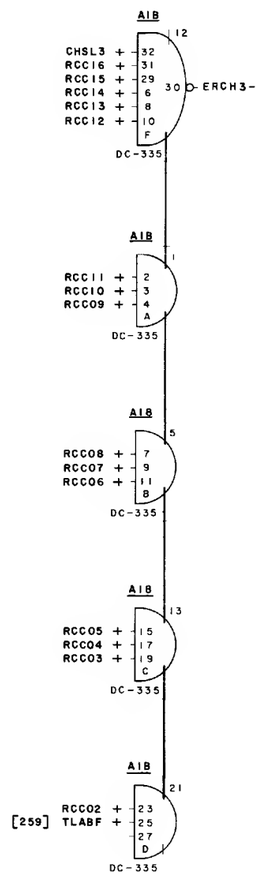
TITLE
DDP-516-21
DMA CHANNEL #3
RANGE COUNTER

SIZE C | DWG NO. 016369 | REV. C

L.B.D. NO. 0.257







NOTES:

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REV.	REVISIONS	CHK
B	ECO 4237	EJK
	REDRAWN. NO CHG	
	2 28 67	

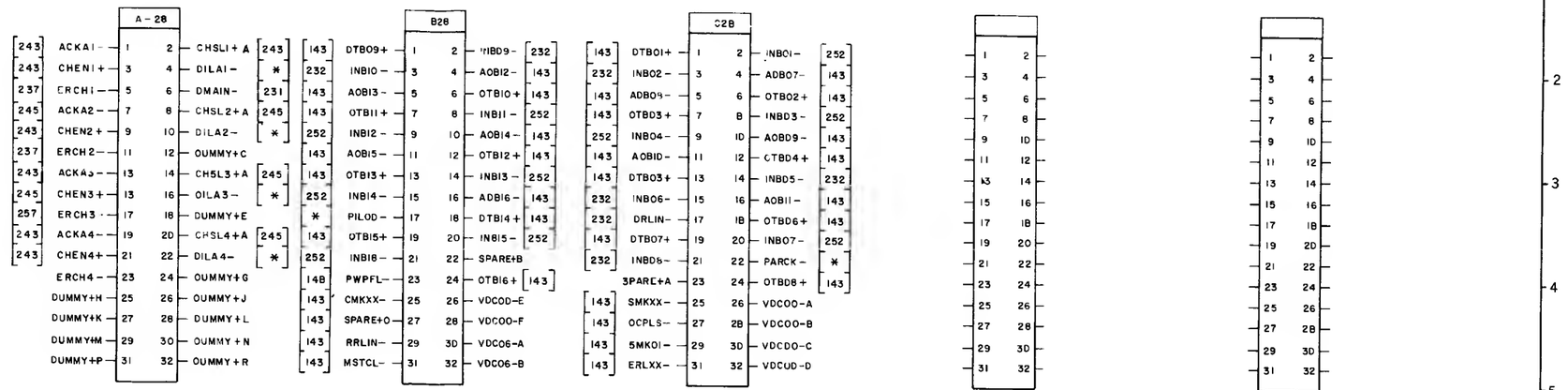
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass.

DR. A. Kurtzer	DATE 1/18/67
ENG.	
APP.	
PROJECT NO. 55215	

TITLE
DDP-516-21
DMA END-OF-RANGE CONTROL

SIZE	DWG NO.	REV.
C	016370	B

L.B.D. NO. 0.259



[*] THESE SIGNALS ARRIVE BY BUS FROM I/O OPTIONS, DEPENDING ON SYSTEM CONFIGURATIONS

REVISIONS

C	ECN 1353		

3C	COMPUTER CONTROL COMPANY, INC
	FRAMINGHAM MASS LOS ANGELES 64 CALIF
DR. S. GREENSTREET	DATE 10 6 66
ENG.	
APP.	
PROJECT NO. 55215	

TITLE: DMA CABLES

SIZE C | DWG NO. 016371 | REV. A

APPENDIX
PAC DESCRIPTIONS

Descriptions of PACs CC-152 and CC-154 follow.

TRANSFER GATE PAC, MODEL CC-152

GENERAL

The Transfer Gate PAC, Model CC-152 (Figure 1), contains 14 2-input NAND gates without collector resistors arranged in four independent groups. Two of the groups contain four NAND gates each with one input being common to the four gates. The other two groups contain three NAND gates each with one input being common to the three gates. All fourteen circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

The Model CC-152 PAC can be used for the common transfer control of up to 14 data signals with the common input used as a control or strobe input. Turn-on rise time is controlled so as to have a guaranteed minimum of 50 nsec with no load.

SPECIFICATIONS

Frequency of Operation

DC to 5 mc (max)

Input Loading

Individual inputs: 1 unit load each

Common inputs: 1 unit load per gate

Output Drive Capability

8 unit loads

Circuit Delay

120 nsec (max) turn on
40 nsec (max) turn off

Current Requirements

+6v: 95 ma

Power Dissipation

560 mw (max)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
C2-C15	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 10 pf ±10%, 100 vdc	930 173 204
M1-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001

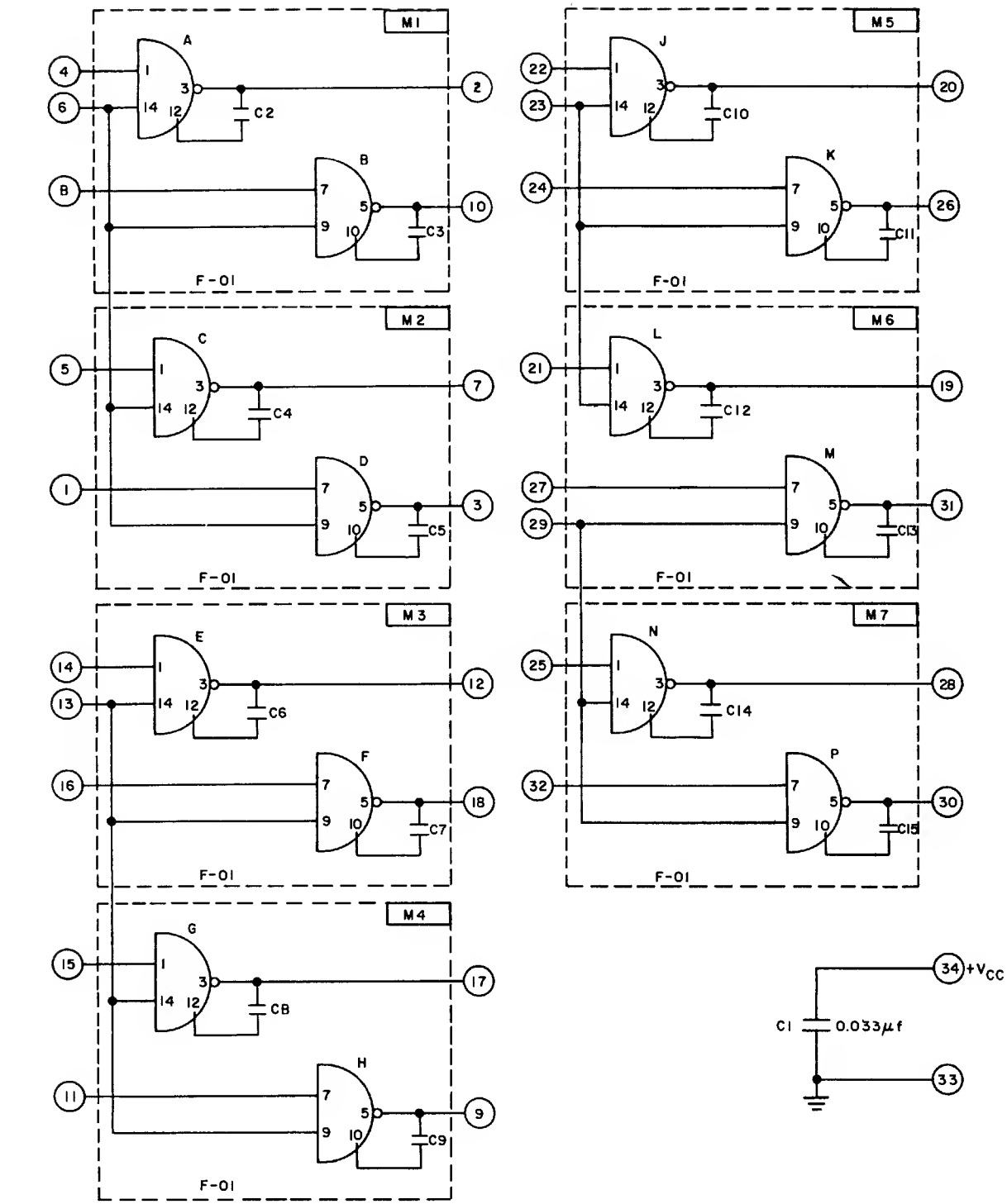


Figure 1. Transfer Gate PAC, Model CC-152, Schematic Diagram

TERMINATION PAC, MODEL CC-154

The Termination PAC, Model CC-154 (Figure 1), contains 27 diode clamp circuits to prevent input signals from overshooting below ground. In addition, the PAC has eight inputs which have 1K resistors connected from input pins to +6 volts.

SPECIFICATIONS:

Frequency of Operation

5 mc

Current Requirements

+6v: 50 ma

Input Loading

Inputs with resistors: 3 unit loads
Inputs without resistors: 0 unit loads

Power Dissipation

300 mw (max.)

Electrical Parts List

Ref. Desig.	Description	3C Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μf ±20%, 50 vdc	930 313 016
CR1-CR27	DIODE	943 024 002
R1-R8	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4w	932 007 049

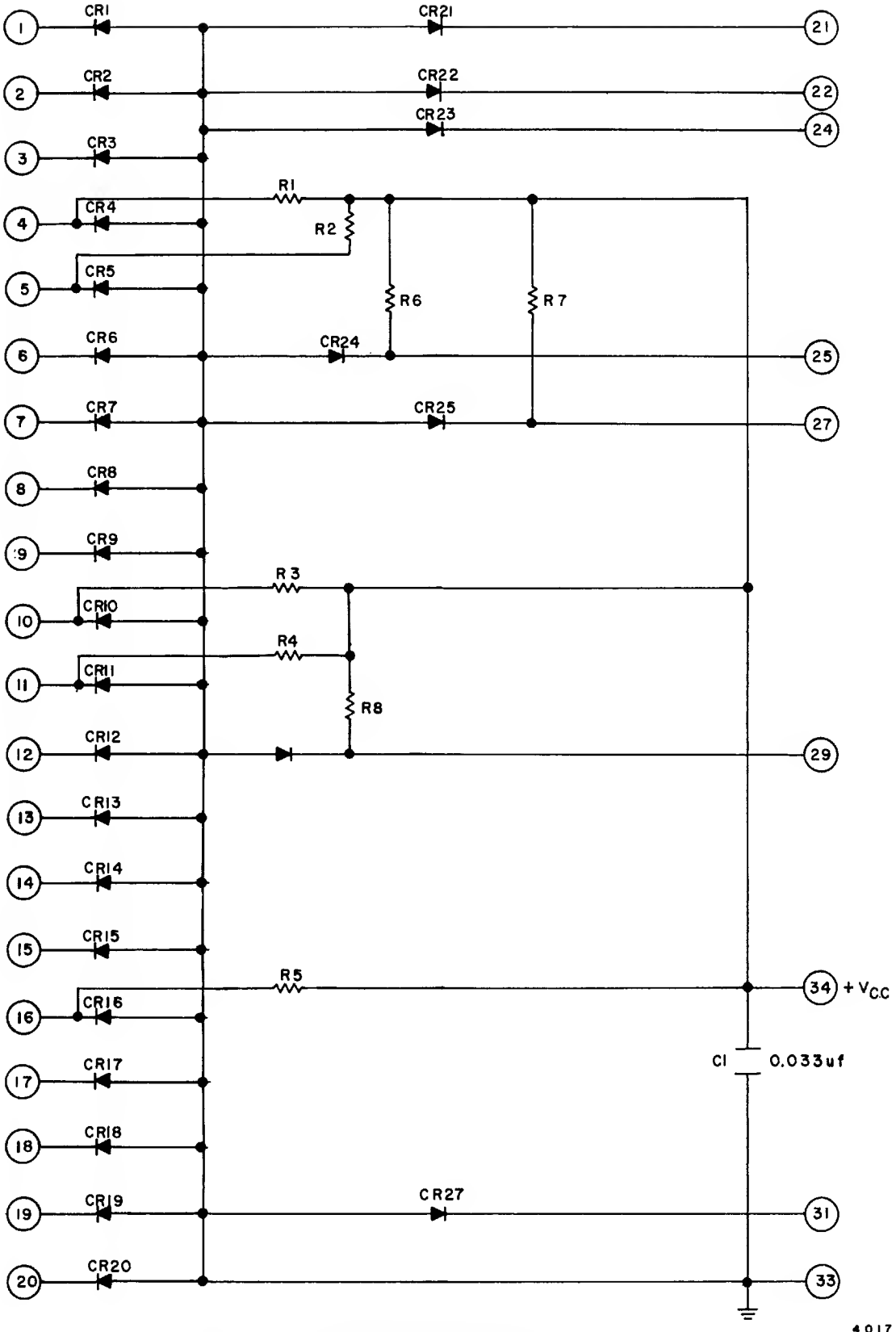


Figure 1. Termination PAC, Model CC-154, Schematic Diagram